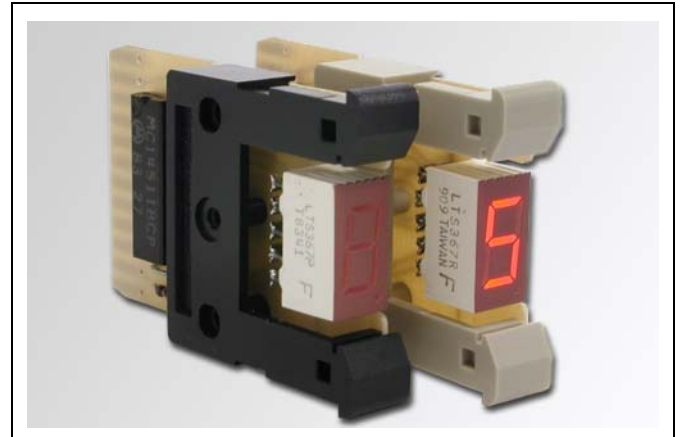


Data Sheet

7-Segment-LED-Displays Codicount, Series 300

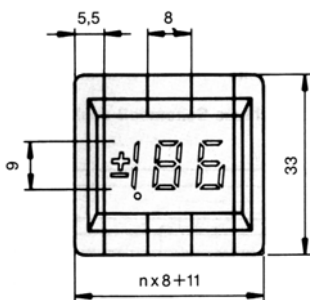
- Single digit red 7-segment LED display
- Character size 9 mm, right hand decimal point
- Module width 8 mm
- Contrast filters for 1 to 4 modules
- Compatible in size with Multiswitch U
- Simple push-fit assembly



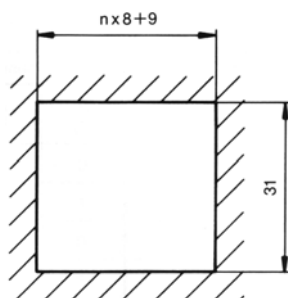
Dimensions

Width	8 mm
Height	33 mm
Character height	9 mm
Depth behind panel	
Type 301, 302, 304, 305	49 mm
Type 315, 316	64 mm

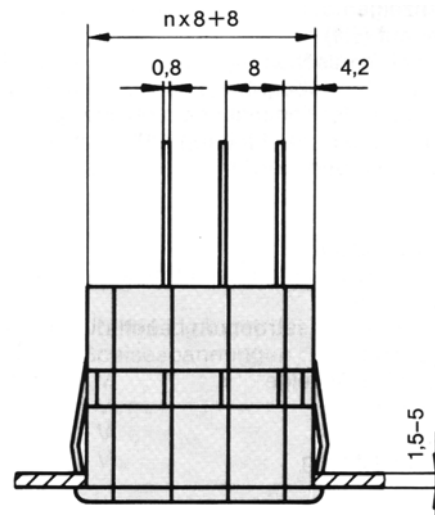
Front-view



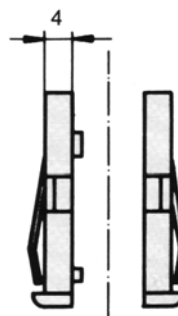
Panel cut-out



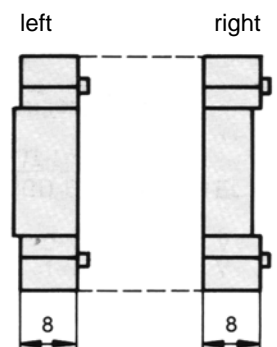
Top view



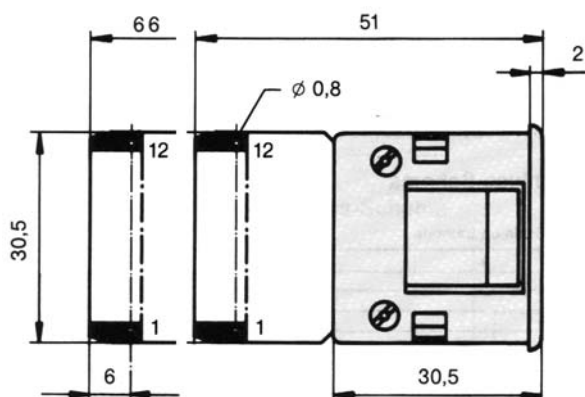
End bracket pair



Thumbwheel switch adapters



Side view



General data

Depending on the type and series involved, the modules are available with TTL or CMOS logic. The program also includes modules with matching elements for expanded supply voltage ranges.

The 7-Segment-LED-Displays with character heights of 9 mm, 16 mm, 25 mm, 35 mm and 45 mm feature parallax-free reading.

The individual modules are 8 mm, 10 mm, 20 mm and 40 mm wide. They can be assembled to form blocks of any size. They are particularly suitable for combination assemblies with the Multiswitches.

Low-power-Schottky logic (LS-TTL) is used in various TTL modules to reduce the supply current.

The inputs of the CMOS modules in series 800 are terminated with resistors. This puts non-used or non-connected inputs on a defined potential level.

The following logic condition definitions apply in the descriptions:

logic 0 = «0» = «L» = $0\text{ V} - U_{in}$ «0» max
 logic 1 = «1» = «H» = U_{in} «1» min – V_{CC}

The following functions generally apply to decoders:

- LT (Lamp Test) When this input is set to «0», the character 8 will appear. This instruction is used to check the proper function of the segments.
- RBI (Ripple Blanking Input) This instruction is used to automatically blank zeros over an arbitrary number of digits. If this terminal is on «0» and if the BCD value is also «0000», the display will be blank.
- BI (Blanking Input) (for CMOS only) If this input is set to «0», the display will extinguish and overwrite all other available information with the exception of the «LT» instruction. Brightness control can be achieved by a clock with variable pulse width.
- RBO/BI (for TTL only) This terminal can be used either as an output or input.
RBO (ripple blanking output)
 For zero blanking, this output is connected with the «RBI» terminal of the next lower decade.
BI (blanking input)
 This input operates in a manner similar to the input for CMOS logic modules; it overwrites **all** other instructions. The basic distinction is in the control mode. Since this terminal can be an input or an output, access must be via integrated circuits with **open collectors**. Termination resistances should not be used, because they are already contained in the decoder. If this function is not needed, the terminal **must** remain open.

General technical data

	TTL	CMOS
Maximum permissible ambient temperature ¹⁾	0 °C ... +50 °C	0 °C ... +50 °C
Supply voltage V_{CC} *	+5 C ± 5 %	+ 5 V ± 5 % + 10 V ± 10 % + 12 V ± 10 % + 15 V ± 10 %
Count frequency	≤ 5 MHz	≤ 100 kHz

1) Separate or forced ventilation must be provided if the temperature increases beyond the specified limit.

	TTL	CMOS
Input voltage U_{in}	max. 5.5 V	max. $V_{CC} + 0.5\text{ V}$
Rise and fall time on pulses	max. 40 ns	max. 15 µs
Pulse width	min. 50 ns	min. 1 µs

* Only the term V_{CC} is used for TTL and CMOS supply in all data and circuit diagrams.

All further deviating data are listed in the descriptions of the individual modules.

IMPORTANT

General handling directions

When using components in CMOS logic the strict observation of the following points are indispensable:

- Persons and equipment must be earthed.
- The relative humidity should be within the range between 40 and 50 %.
- Do not touch elements beyond the housing.
- The conductive rubber on the connector should not be removed but immediately before plug-in.
- Modules which are not incorporated in a circuitry have to be connected by conductive rubber with the connector.
- Modules in CMOS logic should be mounted in a circuit in the end.
- All inputs not used should be put to GND or V_{CC} .
- The maximum signal voltage should never be exceeded (see general technical data).
- Do never connect any outputs to V_{CC} or GND.
- Do not exceed the maximum values of the supply voltage (see general technical data).

Order Number Configuration

① Series	Series 300	3
② Type	Type 301	01
	Type 302	02
	Type 304	04
	Type 305	05
	Type 315	15
	Type 316	16
③ Display	red	0
④ Logics	TTL	1
	C-MOS	2
	without logics, CA	3
	without logics, CC	4
	with adaptation	5
⑤ Supply voltage	+5 V	0
	+10V	4
	+12 V	5
	+15 V	6
	+24 V	7
⑥ Colour of housing	grey	1
	black	2
⑦ Connection	plug in	1

Ordering Key

①	②	③	④	⑤	⑥	⑦
3		0				1

- ① Series 300
- ② Type
- ③ Display red
- ④ Logics
- ⑤ Supply voltage
- ⑥ Colour of housing
- ⑦ Plug in connection

Accessories

Codicounts and/or Multiswitches can be assembled to blocks with the following accessories. Based on customer specification, Crameda provides block assembly of Codicount and Multiswitch to "ready to install" units. For details see section block assembly.

Blank Spacing Module



A blank spacing module can be placed in any position within the display assembly. A blank spacing module has the same dimension as a display module.

Order No. 1 piece	Colour of housing		Front frame width	Module width
300-01-101	grey		8 mm	8 mm
300-01-102	black			

Division Modules



If Codicounts and Multiswitches are joined to a block, division modules must be used.

Order No. 1 piece	Colour of housing	Assembly	Front frame width	Module width
300-04-311	grey	left side of the display	8 mm	8 mm
300-04-312	black			
300-04-321	grey	right side of the display		
300-04-322	black			

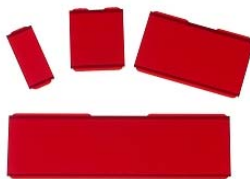
End Brackets



Ready to install blocks are formed by plugging together display modules and left and right end brackets. Spring catches locate the block in the front panel.

Order No. 1 pair	Colour of housing	Front panel thickness	Front frame width	Module width
300-03-301	grey	1.5 – 5 mm	5.5 mm	4 mm
300-03-302	black			

Contrast Filter

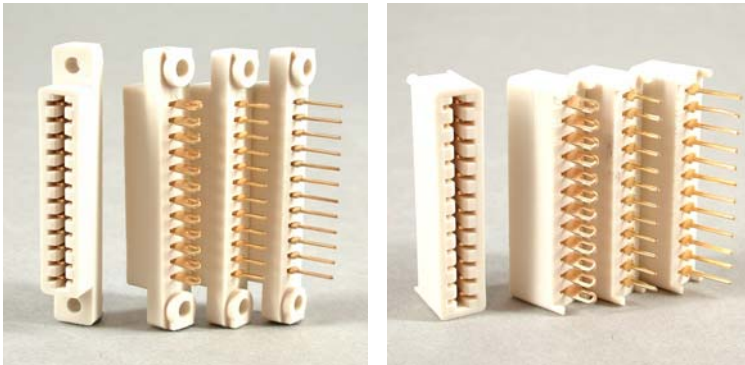


Contrast filters are available for 1 to 4 decades.

Order No. 1 piece	Number of Decades	Length
300-06-008	1	8 mm
300-06-016	2	16 mm
300-06-024	3	24 mm
300-06-032	4	32 mm

Plug in Connectors

Connectors are available with or without flange and different soldering pins. Details see Online Catalogue <Plug-in Connectors>.



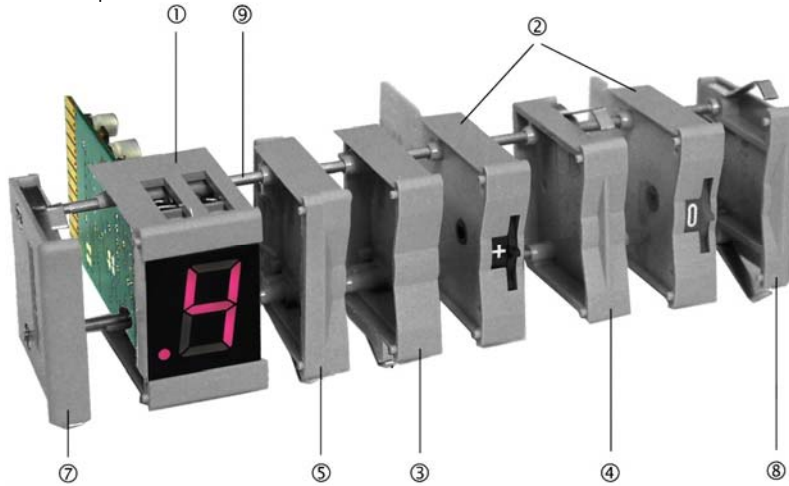
Block Assembly: Mounting of Codicount and Multiswitch

Codicount Series 300 and Multiswitch Range U

Ready to install blocks are built-up by simply plug the individual modules (Codicount, Multiswitch, division module, left and right end brackets) together. The completed blocks are inserted into the cut-out of the front panel. Spring catches locate the block in the front panel.

Based on customer specification, Crameda provides block assembly of Codicount and Multiswitch to "ready to install" units.

Schematic picture



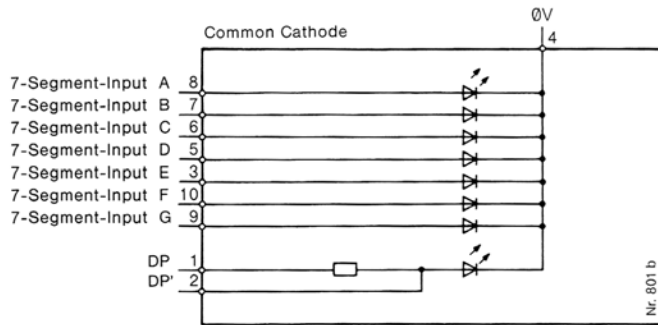
- 1 Codicount
- 2 Multiswitch
- 3 Blank spacing module Multiswitch
- 4 Ribbed division module for Multiswitch
- 5 Division module
- 7 End bracket Codicount*
- 8 End bracket Multiswitch*

* These modules are available in pairs only.

Type 301

- 7-segment display
- Direct input
- 5, 10, 12 or 15 V supply voltage

Circuit diagram

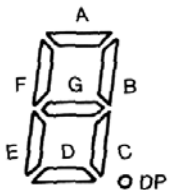


In this display module, all segments are wired directly to the PCB terminations. It is operated with the 7-segment code.

For a fixed decimal point, input DP is connected to $+V_{CC}$ via the built-in current limiting resistor.

For the floating decimal point mode and particularly in multiplex operation, input DP' must be wired to an external driver.

Segment configuration



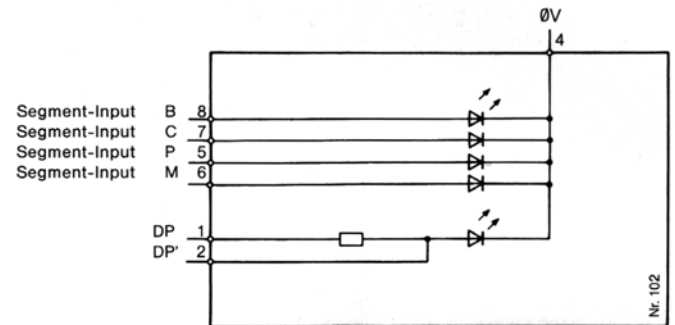
Technical data

Forward voltage of LEDs with $I_{nom} = 6 \text{ mA}$	typ. 1.7 V
Recommended operating current per LED	5-7 mA DC
Inverse voltage	max. 3 V
Character height	9 mm
Depth behind panel	49 mm

Type 302

- Sign and overflow display
- Direct input
- 5, 10, 12 or 15 V supply voltage

Circuit diagram

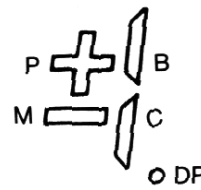


This display is used to indicate sign and overflow (± 1).

For a fixed decimal point, input DP is connected to $+V_{CC}$ via the built-in current limiting resistor.

For the floating decimal point mode and particularly in multiplex operation, input DP' must be wired to an external driver.

Segment configuration



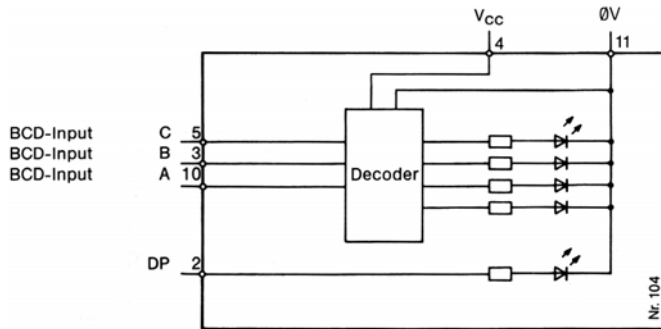
Technical data

Forward voltage of LEDs with $I_{nom} = 6 \text{ mA}$	typ. 1.7 V
Recommended operating current per LED	5-7 mA DC
Inverse voltage	max. 3 V
Character height	9 mm
Depth behind panel	49 mm

Type 304

- ♦ Sign and overflow display
- ♦ BCD-input
- ♦ 5, 10, 12 or 15 V supply voltage

Circuit diagram



This module is used to display sign and overflow (± 1). It is operated with the BCD code in positive logic. All inputs are TTL- or CMOS compatible.

Technical data

Supply current I_{CC}	typ. 24 mA
Character height	9 mm
Depth behind panel	49 mm

Input data

Input voltage (all inputs)		
U_{in} «0» applies to all supply voltages	max.	1 V
U_{in} «1» with $V_{CC} = 5 V$	min.	4 V
U_{in} «1» with $V_{CC} = 10 V$	min.	8 V
U_{in} «1» with $V_{CC} = 12 V$	min.	9.8 V
U_{in} «1» with $V_{CC} = 15 V$	min.	12 V
Input current		
I_{in} «0» with $U_{in} = 1 V$	max.	0.1 μA
I_{in} «1» with $U_{in} = 4 V$	max.	16 μA
I_{in} «1» with $U_{in} = 8 V$	max.	17 μA
I_{in} «1» with $U_{in} = 9.8 V$	max.	17 μA
I_{in} «1» with $U_{in} = 12 V$	max.	19 μA

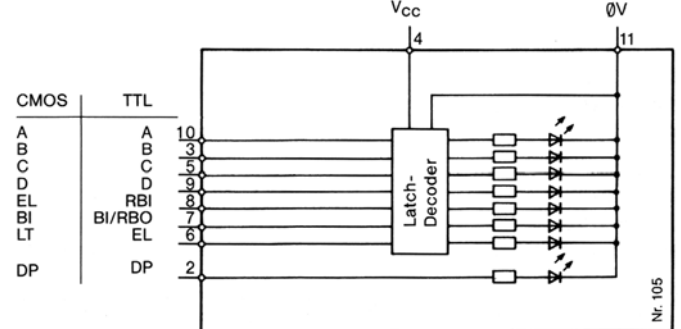
Truth table

Inputs			Outputs
C	B	A	Display
2^2	2^1	2^0	
0	0	0	none
0	0	1	—
0	1	0	7
0	1	1	-7
1	0	0	+
1	0	1	\pm
1	1	0	+7
1	1	1	± 7 (Test)

Type 305

- ♦ 7-segment display
- ♦ BCD-input
- ♦ Memory
- ♦ 5, 10, 12 or 15 V supply voltage

Circuit diagram



In this module, the display is operated by the BCD code in positive logic. A control signal (Input EL) makes it possible to freeze the display and suppress response to changing BCD input signals.

Caution: These terminals for TTL and CMOS are not identical. Observe the General handling directions for CMOS logic elements (s. page Fehler! Textmarke nicht definiert.).

Technical data

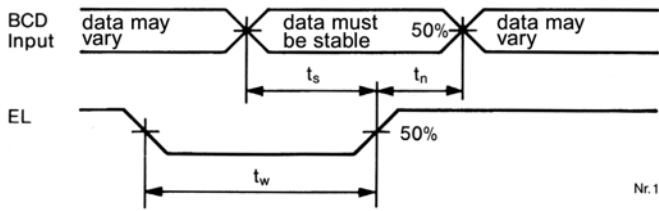
Supply current I_{CC} for TTL	typ. 93 mA
for CMOS	typ. 48 mA
Character height	9 mm
Depth behind panel	49 mm

Input data

Input voltage (all inputs)		
U_{in} «0» with $V_{CC} = 5 V$	max. 0.8 V	1.5 V
U_{in} «0» with $V_{CC} = 10 V$	max.	3 V
U_{in} «0» with $V_{CC} = 12 V$	max.	3.6 V
U_{in} «0» with $V_{CC} = 15 V$	max.	4.5 V
U_{in} «1» with $V_{CC} = 5 V$	min. 2 V	3.5 V
U_{in} «1» with $V_{CC} = 10 V$	min.	7 V
U_{in} «1» with $V_{CC} = 12 V$	min.	8.4 V
U_{in} «1» with $V_{CC} = 15 V$	min.	10.5 V

Input currents TTL logic:

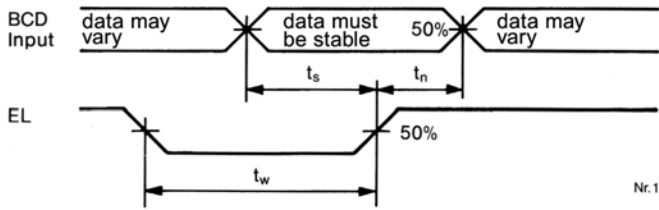
BCD-Inputs with EL = «0»	
I_{in} «0» with $U_{in} = 0.4 V$	max. -1.6 mA
I_{in} «1» with $U_{in} = 2.4 V$	max. 80 μA
With EL = «1» I_{in} «0» and «1»	max. -0.1 mA
Inputs EL and RBI	
I_{in} «0» with $U_{in} = 0.4 V$	max. -1.6 mA
I_{in} «1» with $U_{in} = 2.4 V$	max. 40 μA
Input BI	
I_{in} «0» with $U_{in} = 0.4 V$	max. -3.2 mA
I_{in} «1» with $U_{in} = 2.4 V$	max. 80 μA



Length of storage instruction t_w min. 45 ns
 Length of setting time t_s min. 30 ns
 Length of holding time t_n min. 0 ns

Input currents CMOS logic:

all inputs
 $I_{in} \llcorner 0 \gg$ and $I_{in} \llcorner 1 \gg$ typ. 10 pA
 Input capacitance C_{in} typ. 5 pF



	V_{CC}		
Length of storage instruction	t_w 5	min.	400 ns
	10	min.	160 ns
	15	min.	100 ns
Length of setting time	t_s 5	min.	150 ns
	10	min.	70 ns
	15	min.	40 ns
Length of holding time	t_n 5	min.	75 ns
	10	min.	35 ns
	15	min.	20 ns

Output data (RBO only)

Output voltage
 $U_{out} \llcorner 0 \gg$ with $I_{out} = -3.2$ mA max. 0.4 V
 $U_{out} \llcorner 1 \gg$ with $I_{out} = -80$ μ A min. 2.4 V
 Output current
 $I_{out} \llcorner 0 \gg$ max. -3.2 mA
 $I_{out} \llcorner 1 \gg$ max. -80 μ A

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch): This instruction will freeze the display and suppress further response to changes of the BCD input.

- «EL» on «0» The display responds to the BCD input value.
- «EL» on «1» The display freezes on the last value.

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

- «DP» on «0» Decimal point off
- «DP» on «1» Decimal point on

Truth table CMOS logic

Inputs							Outputs
EL	LT	D 2 ³	C 2 ²	B 2 ¹	A 2 ⁰	BI	Display
x	0	x	x	x	x	x	8 (Test)
x	1	x	x	x	x	0	none
0	1	0	0	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	0	1	0	1	2
0	1	0	0	1	1	1	3
0	1	0	1	0	0	1	4
0	1	0	1	0	1	1	5
0	1	0	1	1	0	1	6
0	1	0	1	1	1	1	7
0	1	1	0	0	0	1	8
0	1	1	0	0	1	1	9
1	1	x	x	x	x	1	stored*

x = «0» or «1»

* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Truth table TTL logic

Inputs							Outputs	
EL	RBI	D 2 ³	C 2 ²	B 2 ¹	A 2 ⁰	BI**	RBO	Display
x	x	x	x	x	x	0	0	none
0	0	0	0	0	0	x	0	none
0	1	0	0	0	0	1	1	0
0	x	0	0	0	1	1	1	1
0	x	0	0	1	0	1	1	2
0	x	0	0	1	1	1	1	3
0	x	0	1	0	0	1	1	4
0	x	0	1	0	1	1	1	5
0	x	0	1	1	0	1	1	6
0	x	0	1	1	1	1	1	7
0	x	1	0	0	0	1	1	8
0	x	1	0	0	1	1	1	9
0	x	1	0	1	0	1	1	A
0	x	1	0	1	1	1	1	b
0	x	1	1	0	0	1	1	c
0	x	1	1	0	1	1	1	d
0	x	1	1	1	0	1	1	e
0	x	1	1	1	1	1	1	f
1	x	x	x	x	x	1	1	stored*

x = «0» or «1»

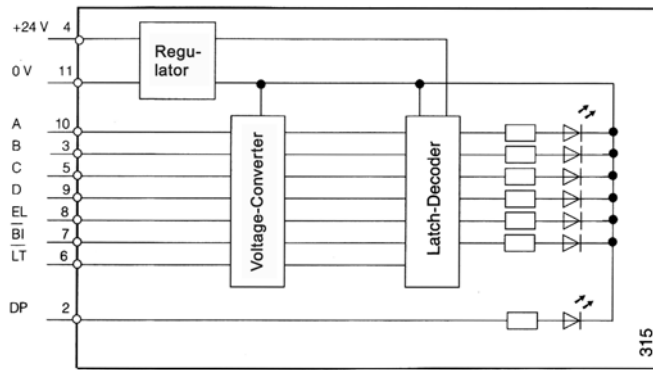
* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

** Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 315

- ♦ 7-segment display
- ♦ BCD-input
- ♦ Memory
- ♦ 24 V signal and supply voltage

Circuit diagram



In this module, the display is controlled by the BCE code in positive logic. The signal voltage is + 24 V. A control signal (input EL) will freeze the display without affecting incoming BCD signals.

Technical data

Supply voltage V_{CC}	20-30 V
Supply current I_{CC} with $V_{CC} = 20-30 V$	typ. 30 mA
Signal voltage	20-30 V
Limit frequency with $V_{CC} = 20-30 V$	≤ 50 kHz
Character height	9.2 mm
Depth behind panel	64 mm

Input data without DP

Input voltage (all inputs)		
$U_{in} \langle 0 \rangle$	min. -30 V	max. +5 V
$U_{in} \langle 1 \rangle$	min. +19 V	max. +30 V
Input currents (all inputs)		
$I_{in} \langle 0 \rangle$ with $U_{in} = -0.5 V$	max. -30 μ A	
$U_{in} = +5 V$	max. +0.25 mA	
$I_{in} \langle 1 \rangle$ with $U_{in} = +19 V$	max. +0.88 mA	
$U_{in} = +30 V$	max. +1.5 mA	
All inputs open = logical $\langle 0 \rangle$		
Input resistance (all inputs)	≈ 20 k Ω	

Decimal point (DP): The decimal point must be controlled externally. There is an integral limiting resistor.

- «DP» on $\langle 0 \rangle$ Decimal point off
- «DP» on $\langle 1 \rangle$ Decimal point on

Input supply (DP)

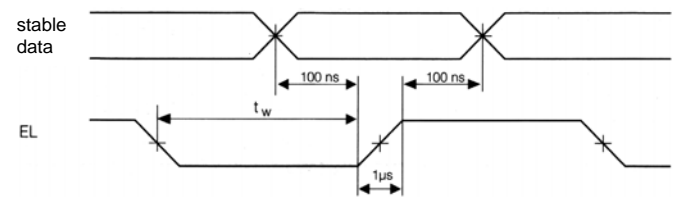
$U_{in} \langle 0 \rangle$	min. -0.5 V	max. +1.5 V
$U_{in} \langle 1 \rangle$	min. +19 V	max. +30 V

Input currents (DP)

$I_{in} \langle 0 \rangle$ with $U_{in} = -0.5 V$	max. -1 mA
$U_{in} = +1.5 V$	max. +30 μ A
$I_{in} \langle 1 \rangle$ with $U_{in} = +19 V$	max. +3 mA
$U_{in} = +30 V$	max. +5 mA

Switching times

Length of storage instruction t_w min. 160 ns



Truth table

Inputs							Outputs
LT	BI	EL	D 2 ³	C 2 ²	B 2 ¹	A 2 ⁰	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
0	1	x	x	x	x	x	8 (Test)
1	0	x	x	x	x	x	none
1	1	1	x	x	x	x	stored*

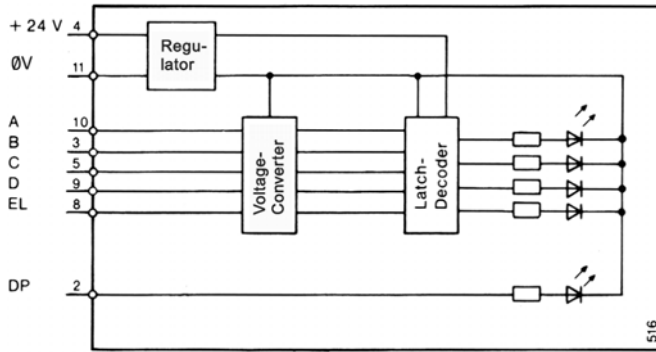
x = $\langle 0 \rangle$ or $\langle 1 \rangle$

* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Type 316

- ♦ Sign and overflow display
- ♦ BCD-input
- ♦ Memory
- ♦ 24 V signal and supply voltage

Circuit diagram



This module is used to display sign and overflow (± 1). It is controlled with the BCD code in positive logic.

The signal and display voltage is +24 V. A control signal (input EL) will freeze the display without affecting incoming BCD signals.

Technical data

Supply voltage V_{CC}	18-30 V
Supply current I_{CC} with $V_{CC} = 18-30$ V	typ. 40 mA
Signal voltage	11-30 V
Limit frequency with $V_{CC} = 18-30$ V	≤ 50 kHz
Character height	9.2 mm
Depth behind panel	64 mm

Input data without DP

Input voltage (all inputs)	
$U_{in} \langle 0 \rangle$	min. -0.5 V max. +5 V
$U_{in} \langle 1 \rangle$	min. +11 V max. +30 V
Input currents (all inputs)	
$I_{in} \langle 0 \rangle$ with $U_{in} = -0.5$ V	max. -30 μ A
$U_{in} = +5$ V	max. +0.25 mA
$I_{in} \langle 1 \rangle$ with $U_{in} = +11$ V	max. +0.55 mA
$U_{in} = +30$ V	max. +1.5 mA
Open inputs = logical $\langle 0 \rangle$	
Input resistance (all inputs)	≈ 20 k Ω

Decimal point (DP): The decimal point must be controlled externally. There is an integral limiting resistor.

- «DP» on $\langle 0 \rangle$ Decimal point off
- «DP» on $\langle 1 \rangle$ Decimal point on

Input supply

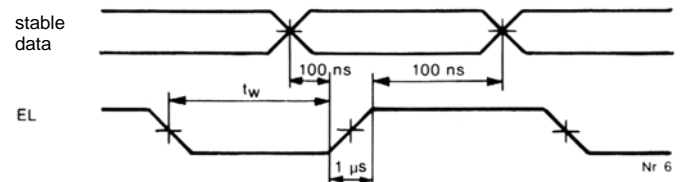
$U_{in} \langle 0 \rangle$	min. -0.5 V max. +1.5 V
$U_{in} \langle 1 \rangle$	min. +5 V max. +30 V

Input currents (DP)

$I_{in} \langle 0 \rangle$ with $U_{in} = -0.5$ V	max. -1 mA
$U_{in} = +1.5$ V	max. +30 μ A
$I_{in} \langle 1 \rangle$ with $U_{in} = +5$ V	max. +2 mA
$U_{in} = +30$ V	max. +10 mA

Switching times

Length of storage instruction t_w min. 160 ns



Truth table

Inputs					Outputs
EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
0	0	0	0	0	\pm
0	0	0	0	1	-
0	0	0	1	0	\pm
0	0	0	1	1	\pm
0	0	1	0	0	-
0	0	1	0	1	+
0	0	1	1	0	+
0	0	1	1	1	\pm
0	1	0	0	0	\pm
0	1	0	0	1	\pm
0	1	0	1	0	± 1
0	1	0	1	1	1
0	1	1	0	0	+1
0	1	1	0	1	-1
0	1	1	1	0	+1
0	1	1	1	1	+1
1	x	x	x	x	stored*

x = $\langle 0 \rangle$ or $\langle 1 \rangle$

* = controlled by applied BCD code during the leading edge of the «EL» instruction signal.