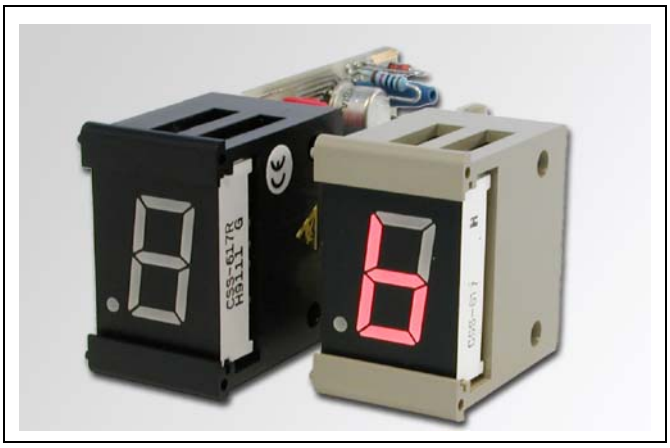
Data Sheet

7-Segment-LED-Displays Codicount, Series 800

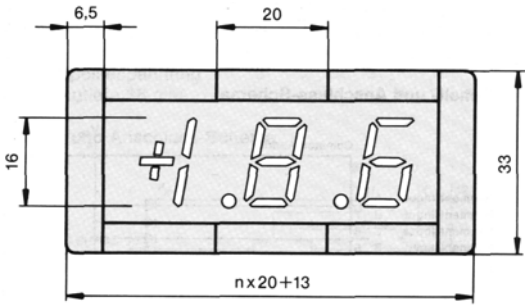


- Single digit red 7-segment LED display
- Character size 16 mm, left hand decimal point
- Module width 20 mm
- Contrast filters for 1 to 6 modules
- Combinable with Multiswitch ranges H, M, R and S

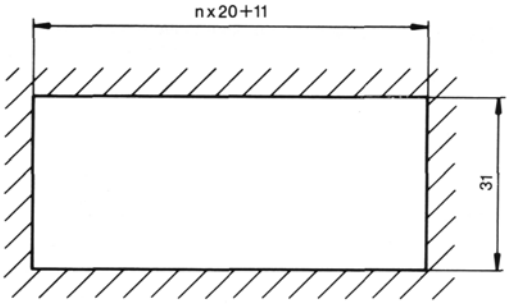
Dimensions

Width	20 mm
Height	33 mm
Character height	16 mm
Depth behind panel	
Type 801, 802, 803, 804, 805, 806	38 mm
Type 809, 811, 815, 816, 845, 854	64 mm
Type 817, 818, 821, 822, 846, 856	74 mm

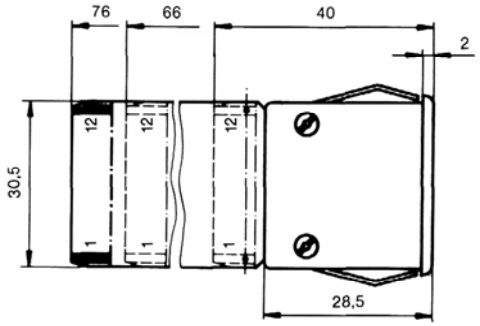
Font view



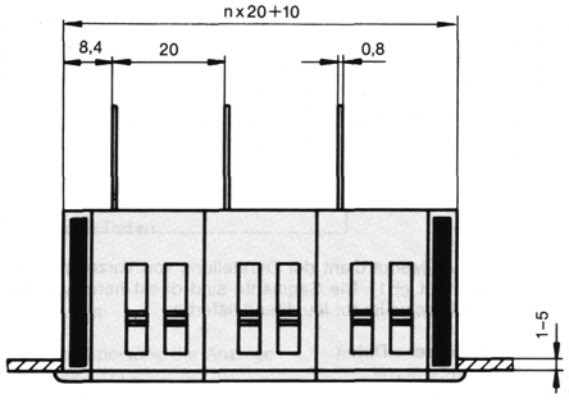
Panel cut-out



Side view

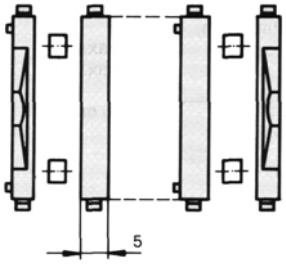


Top view



End bracket pair

Division plates



General data

Depending on the type and series involved, the modules are available with TTL or CMOS logic. The program also includes modules with matching elements for expanded supply voltage ranges.

The 7-Segment-LED-Displays with character heights of 9 mm, 16 mm, 25 mm, 35 mm and 45 mm feature parallax-free reading.

The individual modules are 8 mm, 10 mm, 20 mm and 40 mm wide. They can be assembled to form blocks of any size. They are particularly suitable for combination assemblies with the Multiswitches.

Low-power-Schottky logic (LS-TTL) is used in various TTL modules to reduce the supply current.

The inputs of the CMOS modules in series 800 are terminated with resistors. This puts non-used or non-connected inputs on a defined potential level.

The following logic condition definitions apply in the descriptions:

logic 0 = «0» = «L» = 0 V – U_{in} «0» max
logic 1 = «1» = «H» = U_{in} «1» min – V_{CC}

The following functions generally apply to decoders:

– LT (Lamp Test) When this input is set to «0», the character 8 will appear. This instruction is used to check the proper function of the segments.

– RBI (Ripple Blanking Input)
This instruction is used to automatically blank zeros over an arbitrary number of digits. If this terminal is on «0»and if the BCD value is also «0000», the display will be blank.

– BI (Blanking Input) (for CMOS only)
If this input is set to «0», the display will extinguish and overwrite all other available information with the exception of the «LT» instruction. Brightness control can be achieved by a clock with variable pulse width.

– RBO/BI (for TTL only)
This terminal can be used either as an output or input.
RBO (ripple blanking output)
For zero blanking, this output is connected with the «RBI» terminal of the next lower decade.
BI (blanking input)
This input operates in a manner similar to the input for CMOS logic modules; it overwrites **all** other instructions. The basic distinction is in the control mode. Since this terminal can be an input or an output, access must be via integrated circuits with **open collectors**. Termination resistances should not be used, because they are already contained in the decoder. If this function is not needed, the terminal **must** remain open.

General technical data

	TTL	CMOS
Maximum permissible ambient temperature[1)]	0 °C ... +50 °C	0 °C ... +50 °C
Supply voltage V_{CC} *	+5 C ± 5 %	+ 5 V ± 5 % + 10 V ± 10 % + 12 V ± 10 % + 15 V ± 10 %
Count frequency	≤ 5 MHz	≤ 100 kHz

1) Separate or forced ventilation must be provided if the temperature increases beyond the specified limit.

	TTL	CMOS
Input voltage U_{in}	max. 5.5 V	max. V_{CC} +0.5 V
Rise and fall time on pulses	max. 40 ns	max. 15 µs
Pulse width	min. 50 ns	min. 1 µs

* Only the term V_{CC} is used for TTL and CMOS supply in all data and circuit diagrams.

All further deviating data are listed in the descriptions of the individual modules.

IMPORTANT

General handling directions

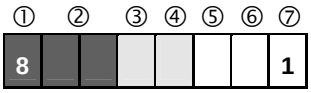
When using components in CMOS logic the strict observation of the following points are indispensable:

- Persons and equipment must be earthed.
- The relative humidity should be within the range between 40 and 50 %.
- Do not touch elements beyond the housing.
- The conductive rubber on the connector should not be removed but immediately before plug-in.
- Modules which are not incorporated in a circuitry have to be connected by conductive rubber with the connector.
- Modules in CMOS logic should be mounted in a circuit in the end.
- All inputs not used should be put to GND or V_{CC}.
- The maximum signal voltage should never be exceeded (see general technical data).
- Do never connect any outputs to V_{CC} or GND.
- Do not exceed the maximum values of the supply voltage (see general technical data).

Order Number Configuration

① **Series**	Series 800	**8**
② **Type**	Type 801	01
	Type 802	02
	Type 803	03
	Type 804	04
	Type 805	05
	Type 806	06
	Type 809	09
	Type 811	11
	Type 815	15
	Type 816	16
	Type 817	17
	Type 818	18
	Type 821	21
	Type 822	22
	Type 845	45
	Type 846	46
	Type 854	54
	Type 856	56
③ **Display**	red	0
	red with sep. anode	3
④ **Logics**	TTL	1
	C-MOS	2
	without logics, CA	3
	without logics, CC	4
	with adaptation	5
⑤ **Supply voltage**	+5 V	0
	+10V	4
	+12 V	5
	+15 V	6
	+24 V	7
⑥ **Colour of housing**	grey	1
	black	2
⑦ **Connection**	plug in	1

Ordering Key



① Series 800
② Type
③ Display
④ Logics
⑤ Supply voltage
⑥ Colour of housing
⑦ Plug in connection

Accessories

Codicounts and/or Multiswitches can be assembled to blocks with the following accessories. Based on customer specification, Crameda provides block assembly of Codicount and Multiswitch to "ready to install" units.
For details see section block assembly.

Blank Spacing Module

A blank spacing module can be placed in any position within the display assembly.
A blank spacing module has the same dimension as a display module.

Order No. 1 piece	Colour of housing	Front panel thickness	Front frame width	Module width
800-01-101	grey	1 – 5 mm	20 mm	20 mm
800-01-102	black			

Division Plates

If Codicounts and Multiswitches are joined to a block, division plates for Codicount and Multiswitche must be used.

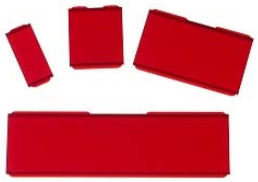
Order No. 1 pair	Colour of housing	Front panel thickness	Front frame width	Module width
800-04-301	grey	1 – 3 mm	5 mm	5 mm
800-04-302	black			
800-04-801	grey	3 – 5 mm		
800-04-802	black			

End Brackets

The display assemblies are completed with end brackets on either side and held together with two threaded rods with slotted nuts. The display assemblies are secured in the front panel by retaining springs.

Order No. 1 pair	Colour of housing	Front panel thickness	Front frame width	Module width
800-03-301	grey	1 – 3 mm	6.5 mm	5 mm
800-03-302	black			
800-03-801	grey	3 – 5 mm		
800-03-802	black			

Contrast Filter



Contrast filters are available for 1 to 6 decades.

Order No. 1 piece	Number of Decades	Length
800-06-020	1	20 mm
800-06-040	2	40 mm
800-06-060	3	60 mm
800-06-080	4	80 mm
800-06-100	5	100 mm
800-06-220	6	120 mm

Threaded Rods

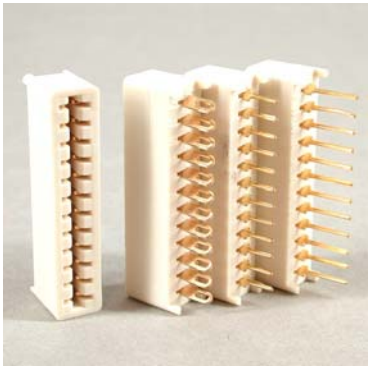
Order No. 1 piece	
G2x LLL mm	LLL = 030 to 250 mm / 2 pieces are required per block.

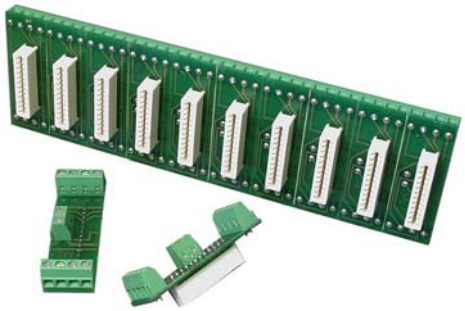
Slotted Nuts

Order No. 1 pair	Order No. 10 pairs	Order No. 50 pairs
M2A002	M2A020	M2A100

Plug in Connectors and Terminal Screw Adapter

Connectors are available with or without flange and different soldering pins.
Terminal screw adapters connect fast and simply the range 800.
Details see Online Catalogue <Plug-in Connectors>.





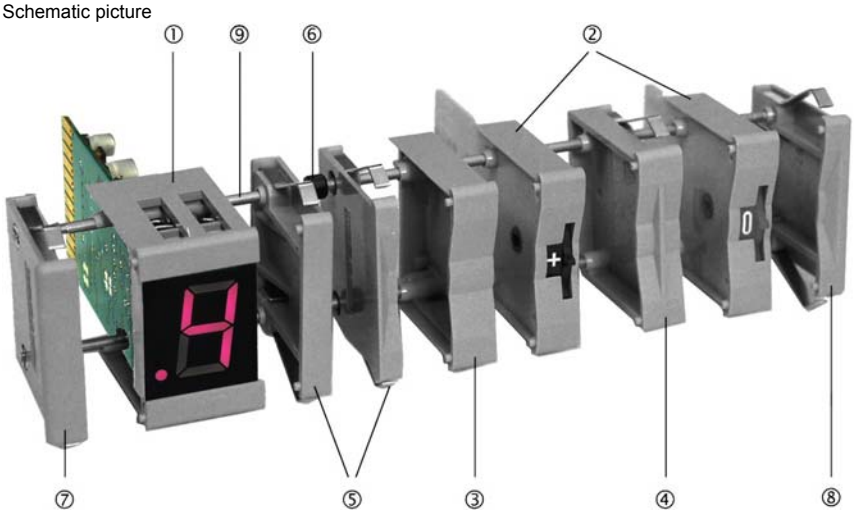
Block Assembly: Mounting of Codicount and Multiswitch

Codicount Series 800 and **Multiswitch Ranges H, M, R and S**

Ready to install blocks are built-up by line up the individual modules (Codicount, Multiswitch, division plates, left and right end brackets). The blocks are secured with threaded rods. The completed blocks are inserted into the cut-out of the front panel. Spring catches locate the block in the front panel.

Based on customer specification, Crameda provides block assembly of Codicount and Multiswitch to "ready to install" units.

Schematic picture



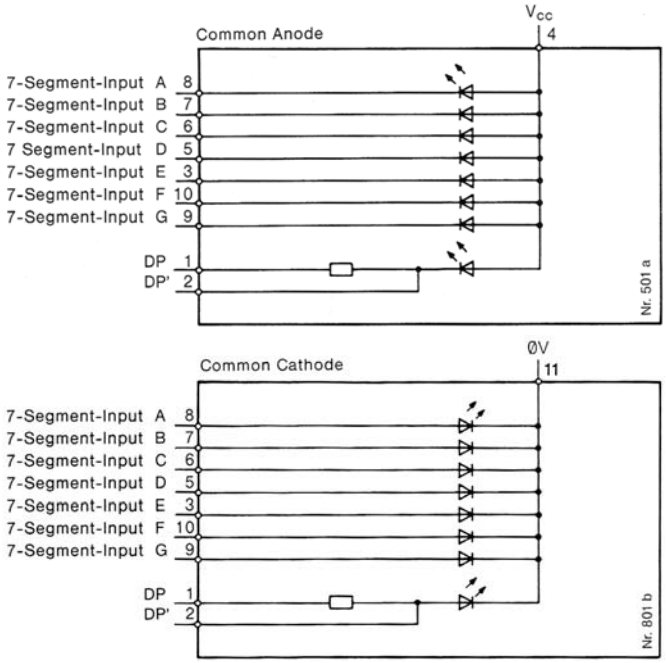
1 Codicount
2 Multiswitch
3 Blank spacing module Multiswitch
4 Ribbed division module for Multiswitch
5 Division plate Codicount*
  Division plate Multiswitch*
6 Guide sleeves for division plates (are included)
7 End bracket Codicount*
8 End bracket Multiswitch*
9 Threaded rods

* These modules are available in pairs only.

Type 801

- 7-segment display
- Direct input
- 5, 10, 12 or 15 V supply voltage

Circuit diagram

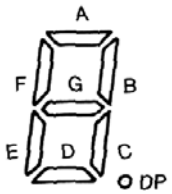


In these display modules, all segments are wired directly to the PCB terminations. They are operated with the 7-segment code.

For a fixed decimal point, input DP is connected directly to 0 volts or via the built-in current limiting resistor, depending on the execution. For the floating decimal point mode and particularly in multiplex operation, input DP' must be wired to an external driver.

The display modules are available with common anode (CA) or with common cathode (CC).

Segment configuration



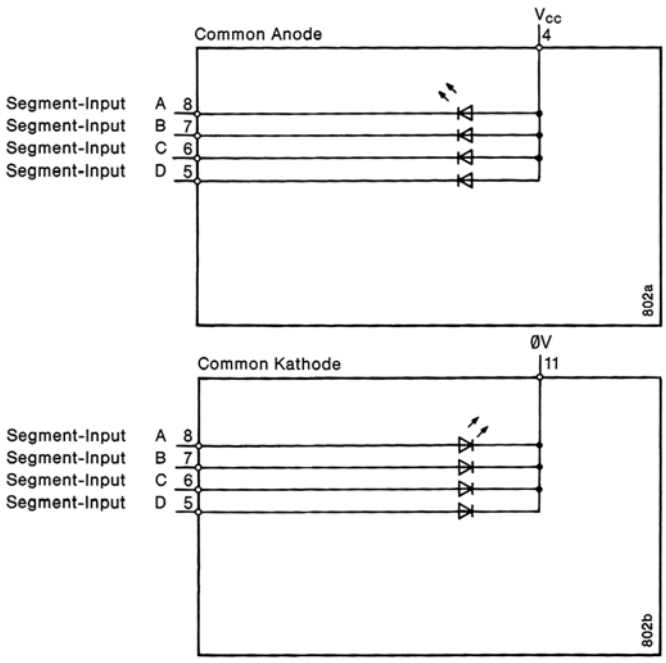
Technical data

Forward voltage of LEDs with $I_{nom.}$	
for segments	typ. 3.4 V
for decimal point	typ. 1.7 V
Recommended operation current per segment	8-12 mA DC
Inverse voltage of LEDs	
for segments	max. 6 V
for decimal point	max. 3 V
Character height	16 mm
Depth behind panel	38 mm

Type 802

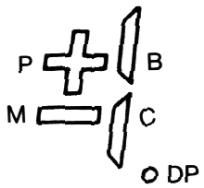
- Sign and overflow display
- Direct input
- 5 V supply voltage

Circuit diagram



This module is used to display sign and overflow (±1). All segments are wired to the PCB terminations.

Segment configuration



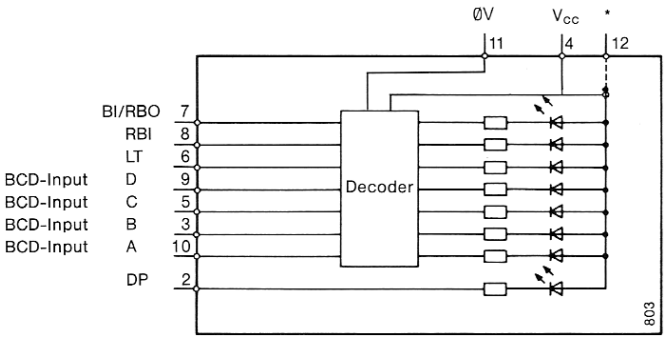
Technical data

Forward voltage of LEDs with I_{nom}	typ. 1.7 V
Recommended operation current per segment	8-12 mA DC
Inverse voltage of LEDs	max. 6 V
Character height	16 mm
Depth behind panel	38 mm

Type 803

- 7-segment display
- BCD input
- TTL logic
- 5 V supply voltage

Circuit diagram



The display in this module is controlled by the BCD code in positive logic.

All inputs and outputs are LS-TTL compatible.

Caution

Terminal 12* can be used to separately power the LED display. However, it must be specified in the order (see ordering data: CA with sep. anode).

Technical data

Supply current	typ. 93 mA
Separate display power terminal (Terminal 12)	+5 V ±20%
Character height	16 mm
Depth behind panel	38 mm

Input data

Input voltage (all inputs)

U_{in} «0»		max.	0.8 V
U_{in} «1»		min.	2 V

Input currents (all inputs except BI)

I_{in} «0» with	U_{in} = 0.4 V	max.	-0.4 mA

Input BI

I_{in} «0» with	U_{in} = 0.4 V	max.	-0.1 mA
I_{in} «1» with	U_{in} = 2.7 V	max.	20 µA

Output data (RBO only)

Output voltage

U_{out} «0» with	I_{out} = 3.2 mA	max.	0.5 V
U_{out} «1» with	I_{out} = -50 µA	min.	2.4 V

Output current

I_{out} «0»	max.	3.2 mA
I_{out} «1»	max.	50 µA

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

«DP» on «0» Decimal point on

«DP» on «1» Decimal point off

Truth table

Inputs							Outputs	
LT	RBI	D 2^3	C 2^2	B 2^1	A 2^0	BI*	RBO	Display
1	1	0	0	0	0	1	1	0
1	x	0	0	0	1	1	1	1
1	x	0	0	1	0	1	1	2
1	x	0	0	1	1	1	1	3
1	x	0	1	0	0	1	1	4
1	x	0	1	0	1	1	1	5
1	x	0	1	1	0	1	1	6
1	x	0	1	1	1	1	1	7
1	x	1	0	0	0	1	1	8
1	x	1	0	0	1	1	1	9
1	0	0	0	0	0	x	0	none
x	x	x	x	x	x	0	0	none
0	x	x	x	x	x	1	1	8 (Test)

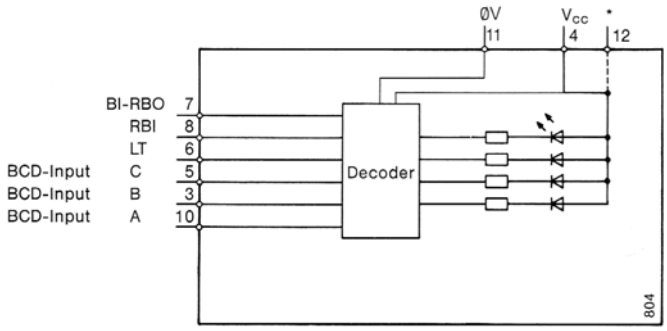
x = «0» or «1»

* Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 804

- Sign and overflow display
- BCD input
- TTL logic
- 5 V supply voltage

Circuit diagram



This module is used to display sign and overflow (±1). It is operated with the BCD code in positive logic. All inputs and outputs are TTL- or CMOS compatible.

Caution

Terminal 12* can be used to separately power the LED display. However, it must be specified in the order (see ordering data: CA with sep. anode).

Technical data

Supply current I_{CC}	typ. 53 mA
Separate display power terminal (Terminal 12)	+5 V ±20%
Character height	16 mm
Depth behind panel	38 mm

Input data

Input voltage (all inputs)			
U_{in} «0»			max. 0.8 V
U_{in} «1»			min. 2 V
Input currents			
BCD input, LT, RBI			
I_{in} «0» with	U_{in} =	0.4 V	max. -0.36 mA
I_{in} «1» with	U_{in} =	2.7 V	max. 20 µA
Input BI			
I_{in} «0» with	U_{in} =	0.4 V	max. -1 mA

Output data (RBO only)

Output voltage	
U_{out} «0»	max. 0.4 V
U_{out} «1»	max. 2.4 V
Output current	
I_{out} «0»	max. 3.2 mA
I_{out} «1»	max. -50 µA

Truth table

Inputs						Outputs	
LT	RBI	C 2^2	B 2^1	A 2^0	BI*	RBO	Display
1	1	0	0	0	1	1	+1
1	x	0	0	1	1	1	–
1	x	0	1	0	1	1	1
1	x	0	1	1	1	1	-1
1	x	1	0	0	1	1	+
1	x	1	0	1	1	1	+1
1	x	1	1	0	1	1	+1
1	x	1	1	1	1	1	–
0	x	x	x	x	1	1	±1 (Test)
1	0	0	0	0	0*	0	none
x	x	x	x	x	0	0	none

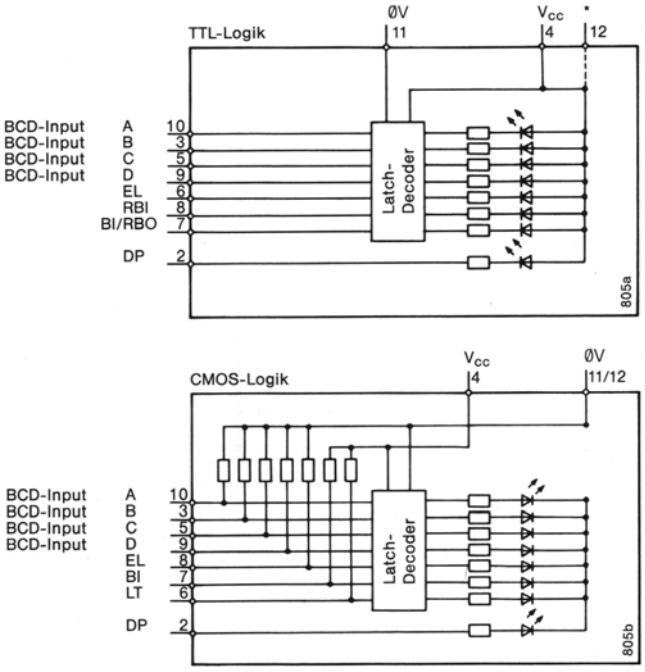
x = «0» or «1»

* Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 805

- 7-segment display
- BCD input
- Memory
- TTL- or CMOS-Logic
- 5, 10, 12 or 15 V supply voltage

Circuit diagram



In this module, the display is operated by the BCD code in positive logic. A control signal (input EL) makes it possible to freeze the display without inhibiting the BCD input signals. TTL and CMOS logic models are available. The inputs of the CMOS model are terminated with resistors.

Caution: The terminals for TTL and CMOS are not identical. Terminal 12* can be used to separately power the LED display in the TTL model. However, it must be specified in the order (see ordering data: CA with sep. anode).

Observe the General handling directions for CMOS logic elements (s. page **Fehler! Textmarke nicht definiert.**).

Technical data

Supply current I_{CC}	
with TTL logic	typ. 140 mA
with CMOS-Logic	typ. 90 mA
Separate display power in TTL model (Terminal 12)	+5 V ±20 %
Character height	16 mm
Depth behind panel	38 mm

Input data

Input voltage (all inputs)

			TTL	CMOS
U_{in} «0» with V_{CC}	=	5 V	max. 0.8 V	1.5 V
	=	10 V	max.	3 V
	=	12 V	max.	3.6 V
	=	15 V	max.	4.5 V
U_{in} «1» with V_{CC}	=	5 V	min. 2 V	3.5 V
	=	10 V	min.	7 V
	=	12 V	min.	8.4 V
	=	15 V	min.	10.5 V

Input currents TTL logic:

BCD input currents with EL = «0»

I_{in} «0» with	U_{in} =	0.4 V	max. -1.6 mA
I_{in} «1» with	U_{in} =	2.4 V	max. 80 µA

With EL = «1»

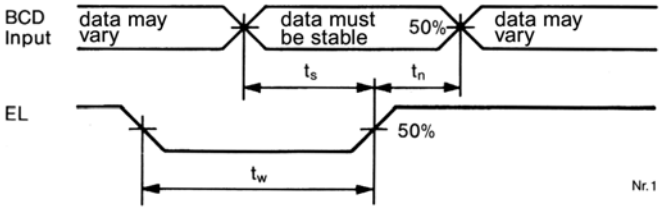
I_{in} «0» and «1»			max. -0.1 mA

Inputs EL and RBI

I_{in} «0» with	U_{in} =	0.4 V	max. -1.6 mA

Input BI

I_{in} «0» with	U_{in} =	0.4 V	max. -3.2 mA
I_{in} «1» with	U_{in} =	2.4 V	max. 80 µA

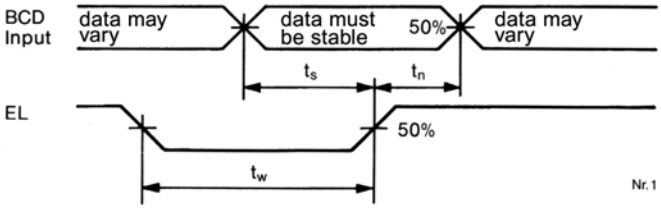


Length of storage instruction	t_w	min.	45 ns
Length of setting time	t_s	min.	30 ns
Length of holding time	t_n	min.	0 ns

Input currents CMOS-Logic

All Inputs Pull-up / Pull-down Resistance 100 kΩ

I_{in} «0» with	U_{in}	= 5 V	max.	15.5 µA
		= 3 V	max.	31 µA
		= 3.6 V	max.	37 µA
		= 4.5 V	max.	46 µA
I_{in} «1» with	U_{in}	= 3.5 V	max.	36 µA
		= 7 V	max.	71.5 µA
		= 8.4 V	max.	86 µA
		= 10.5 V	max.	107 µA



		V_{CC}		
Length of storage instruction	t_w	5	min.	400 ns
		10	min.	160 ns
		15	min.	100 ns
Length of setting time	t_s	5	min.	150 ns
		10	min.	70 ns
		15	min.	40 ns
Length of holding time	t_n	5	min.	75 ns
		10	min.	35 ns
		15	min.	20 ns

Output data (RBO only)

Output voltage

U_{out} «0» with I_{out} =	3.2 mA	max.	0.4 V
U_{out} «1» with I_{out} =	-80 µA	min.	2.4 V

Output current

I_{out} «0»	max.	3.2 mA
I_{out} «1»	max.	-80 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch): This instruction will freeze the display and suppress further response to changes of the BCD input.

- «EL» on «0» The display responds to the BCD input value.
- «EL» on «1» The display freezes on the last value.

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

TTL logic:	«DP» on «0»	Decimal point on.
	«DP» on «1»	Decimal point off
CMOS-Logic:	«DP» on «0»	Decimal point off
	«DP» on «1»	Decimal point on

Truth table CMOS-Logic

Inputs							Outputs
EL	LT	D 2^3	C 2^2	B 2^1	A 2^0	BI	Display
x	0	x	x	x	x	x	8 (Test)
x	1	x	x	x	x	0	none
0	1	0	0	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	0	1	0	1	2
0	1	0	0	1	1	1	3
0	1	0	1	0	0	1	4
0	1	0	1	0	1	1	5
0	1	0	1	1	0	1	6
0	1	0	1	1	1	1	7
0	1	1	0	0	0	1	8
0	1	1	0	0	1	1	9
1	1	x	x	x	x	1	stored *

x = «0» or «1»

* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Truth table TTL logic

Inputs							Outputs	
EL	RBI	D 2^3	C 2^2	B 2^1	A 2^0	BI**	RBO	Display
x	x	x	x	x	x	0	0	none
0	0	0	0	0	0	x	0	none
0	1	0	0	0	0	1	1	0
0	x	0	0	0	1	1	1	1
0	x	0	0	1	0	1	1	2
0	x	0	0	1	1	1	1	3
0	x	0	1	0	0	1	1	4
0	x	0	1	0	1	1	1	5
0	x	0	1	1	0	1	1	6
0	x	0	1	1	1	1	1	7
0	x	1	0	0	0	1	1	8
0	x	1	0	0	1	1	1	9
0	x	1	0	1	0	1	1	A
0	x	1	0	1	1	1	1	b
0	x	1	1	0	0	1	1	C
0	x	1	1	0	1	1	1	d
0	x	1	1	1	0	1	1	E
0	x	1	1	1	1	1	1	F
1	x	x	x	x	x	1	1	stored *

x = «0» or «1 »

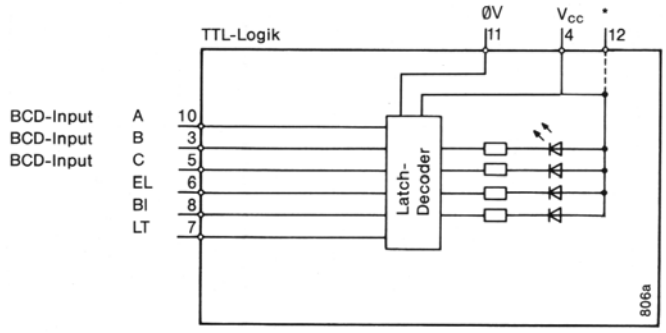
* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

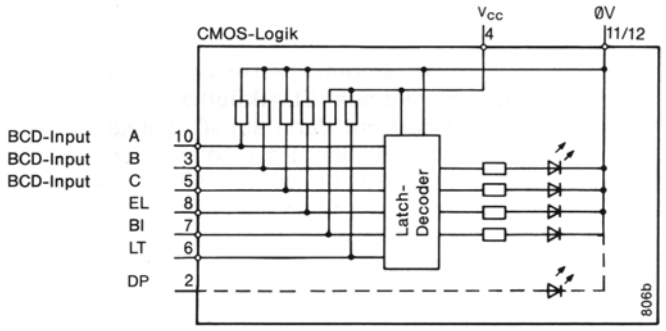
** Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 806

- Sign and overflow display
- Memory
- BCD input
- TTL- or CMOS logic
- 5, 10, 12 or 15 V supply voltage

Circuit diagram





This module is used to display sign and overflow (± 1). The display is operated by the BCD code in positive logic.

A control signal (input EL) makes it possible to freeze the display without inhibiting the BCD input signals. TTL and CMOS logic models are available. The inputs of the CMOS model are terminated with resistors.

Caution: The terminals for TTL and CMOS are not identical. Terminal 12* can be used to separately power the LED display in the TTL model. However, it must be specified in the order (see ordering data: CA with sep. anode).

Observe the General handling directions for CMOS logic elements (s. page **Fehler! Textmarke nicht definiert.**).

Technical data

Supply current I_{CC}	
with TTL logic	typ. 105 mA
with CMOS-Logic	typ. 50 mA
Separate display power terminal in TTL model (Terminal 12)	+5 V ±20 %
Character height	16 mm
Depth behind panel	38 mm

Input data

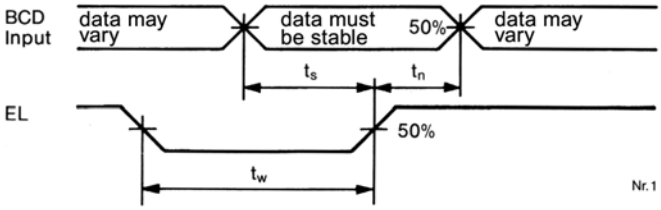
Input voltage (all inputs)

			TTL	CMOS
U_{in} «0» with V_{CC}	=	5 V	max. 0.8 V	1.5 V
	=	10 V	max.	3 V
	=	12 V	max.	3.6 V
	=	15 V	max.	4.5 V
U_{in} «1» with V_{CC}	=	5 V	min. 2 V	3.5 V
	=	10 V	min.	7 V
	=	12 V	min.	8.4 V
	=	15 V	min.	10.5 V

Input currents TTL logic

BCD input currents with EL = «0»

I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	80 µA
With EL = 0 »		
I_{in} «0» and «1»	max.	-0.1 mA
Inputs EL and RBI		
I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	40 µA
Input BI		
I_{in} «0» with U_{in} = 0.4 V	max.	-3.2 mA

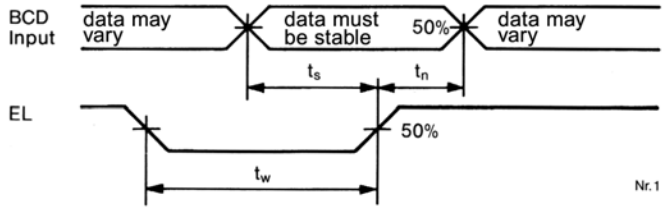


Length of storage instruction	t_w	min. 45 ns
Length of setting time	t_s	min. 30 ns
Length of holding time	t_n	min. 0 ns

Input currents CMOS-Logic

All Inputs Pull-up / Pull-down

Resistance			100 kΩ
I_{in} «0» with U_{in}	= 1.5 V	max.	15.5 µA
	= 3 V	max.	31 µA
	= 3.6 V	max.	37 µA
	= 4.5 V	max.	46 µA
I_{in} «1» with U_{in}	= 3.5 V	max.	36 µA
	= 7 V	max.	71.5 µA
	= 8.4 V	max.	86 µA
	= 10.5 V	max.	107 µA



		V_{CC}	
Length of storage instruction	tw	5	min. 400 ns
		10	min. 160 ns
		15	min. 100 ns
Length of setting time	ts	5	min. 150 ns
		10	min. 70 ns
		15	min. 40 ns
Length of holding time	tn	5	min. 75 ns
		10	min. 35 ns
		15	min. 20 ns

Output data (RBO only)

Output voltage

U_{out} «0» with I_{out} = 3.2 mA max. 0.4 V

U_{out} «1» with I_{out} = -80 µA min. 2.4 V

Output current

I_{out} «0» max. 3.2 mA

I_{out} «1» max. -80 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch): This instruction will freeze the display and suppress further response to changes of the BCD input.

- «EL» on «0» The display responds to the BCD input value.
- «EL» on «1» The display freezes on the last value.

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

TTL logic:
- «DP» on «0» Decimal point on.
- «DP» on «1» Decimal point off

CMOS-Logic:
- «DP» on «0» Decimal point off
- «DP» on «1» Decimal point on

Truth table

Inputs							Outputs	
EL	RBI (TTL only)	C 2^2	B 2^1	A 2^0	LT (CMOS only)	BI**	RBO (TTL only)	Display
x	x	x	x	x	0	1	1	±1 (Test)
x	x	x	x	x	1	0	0	none
0	0	0	0	0	1	0	0	none
0	1	0	0	0	1	1	1	+1
0	x	0	0	1	1	1	1	–
0	x	0	1	0	1	1	1	1
0	x	0	1	1	1	1	1	-1
0	x	1	0	0	1	1	1	+
0	x	1	0	1	1	1	1	+1
0	x	1	1	0	1	1	1	+1
0	x	1	1	1	1	1	1	–
1	x	x	x	x	1	1	1	stored*

x = «0» or «1 »

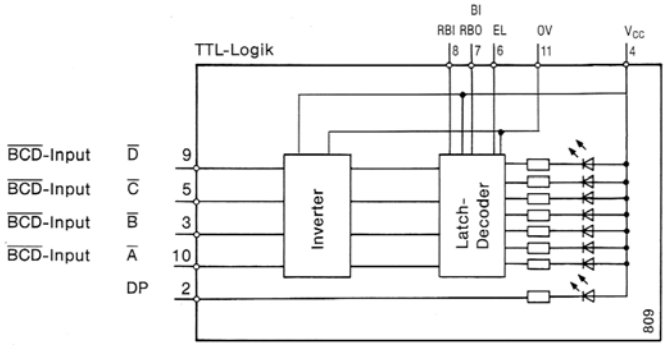
* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

** Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 809

- 7-segment display
- Inverted BCD input
- TTL logic
- 5 V supply voltage

Circuit diagram



In this module, the display is operated with the inverted BCD code in positive logic.

All inputs and outputs are LS-TTL compatible.

Technical data

Supply current I_{cc}	typ. 100 mA
Character height	16 mm
Depth behind panel	64 mm

Input data

Input voltage (all inputs)

U_{in} «0»	max.	0.8 V
U_{in} «1»	min.	2 V

Input currents

BCD input, LT, RBI

I_{in} «0» with U_{in} =	0.4 V	max. -0.36 mA
I_{in} «1» with U_{in} =	2.7 V	max. 20 µA

Input BI

I_{in} «0» with U_{in} =	0.4 V	max. -1 mA

Output data (RBO only)

Output voltage

U_{out} «0» with I_{out} =	-3.2 mA	max. 0.4 V
U_{out} «1» with I_{out} =	-50 µA	min. 2.4 V

Output current

I_{out} «0»	max. 3.2 mA
I_{out} «1»	max. -80 µA

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

«DP» on «0» Decimal point on

«DP» on «1» Decimal point off

Truth table

Inputs							Outputs	
LT	RBI	D 2^3	C 2^2	B 2^1	A 2^0	BI*	RBO	Display
1	1	0	0	0	0	1	1	0
1	x	0	0	0	1	1	1	1
1	x	0	0	1	0	1	1	2
1	x	0	0	1	1	1	1	3
1	x	0	1	0	0	1	1	4
1	x	0	1	0	1	1	1	5
1	x	0	1	1	0	1	1	6
1	x	0	1	1	1	1	1	7
1	x	1	0	0	0	1	1	8
1	x	1	0	0	1	1	1	9
1	0	0	0	0	0	x	0	none
x	x	x	x	x	x	0	0	none
0	x	x	x	x	x	1	1	8 (Test)

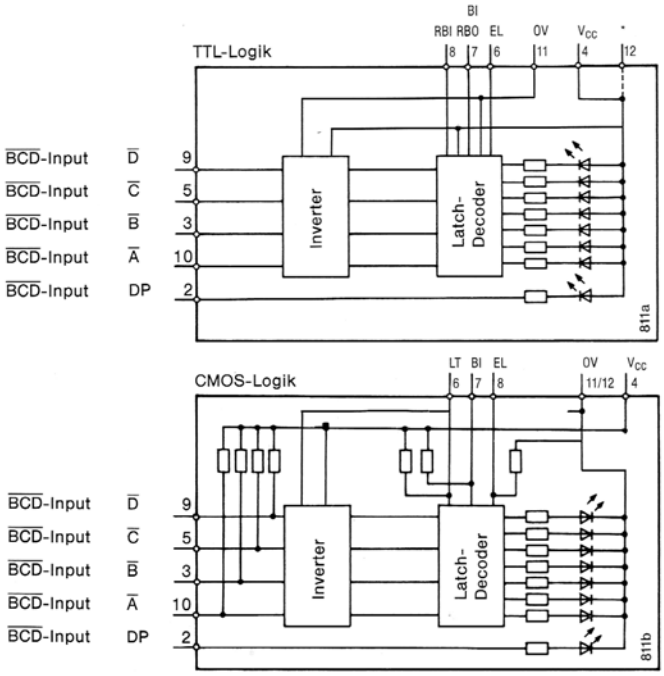
x = «0» or «1 »

* Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 811

- 7-segment display
- Inverted BCD input
- Memory
- TTL- or CMOS-Logic
- 5, 12 or 15 V supply voltage

Circuit diagram



In this module, the display is operated by the inverted BCD code. A control signal (input EL) makes it possible to freeze the display without inhibiting the BCD input signals. The contents of the memory are displayed. TTL and CMOS logic models are available. The inputs of the CMOS model are terminated with resistors.

Caution: The terminals for TTL and CMOS are not identical. Terminal 12* can be used to separately power the LED display in the TTL model. However, it must be specified in the order (see ordering data: CA with sep. anode).

Observe the General handling directions for CMOS logic elements (s. page **Fehler! Textmarke nicht definiert.**).

Technical data

Supply current I_{CC}	
with TTL logic	typ. 105 mA
with CMOS-Logic	typ. 95 mA
Separate display power terminal in TTL model (Terminal 12)	+5 V ±20 %
Character height	16 mm
Depth behind panel	64 mm

Input data

Input voltage (all inputs)

		TTL	CMOS
U_{in} «0» with V_{CC}	= 5 V	max. 0.8 V	1.5 V
	= 12 V	max.	3.6 V
	= 15 V	max.	4.5 V
U_{in} «1» with V_{CC}	= 5 V	min. 2 V	3.5 V
	= 12 V	min.	8.4 V
	= 15 V	min.	10.5 V

Input currents TTL logic

BCD input		
I_{in} «0» with U_{in} = 0.4 V	max.	-0.36 mA
I_{in} «1» with U_{in} = 2.4 V	max.	20 µA
Inputs EL and RBI		
I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	40 µA
Input BI		
I_{in} «0» with U_{in} = 0.4 V	max.	-3.2 mA

Input currents CMOS-Logic

all inputs		
Pull-up / Pull-down Resistance		100 kΩ
I_{in} «0» with U_{in} = 1.5 V	max.	15.5 µA
= 3.6 V	max.	37 µA
= 4.5 V	max.	46 µA
I_{in} «1» with U_{in} = 3.5 V	max.	36 µA
= 8.4 V	max.	86 µA
= 10.5 V	max.	107 µA

Output data (RBO only)

Output voltage		
U_{out} «0» with I_{out} = 3.2 mA	max.	0.4 V
U_{out} «1» with I_{out} = -80 µA	min.	2.4 V
Output current		
I_{out} «0»	max.	3.2 mA
I_{out} «1»	max.	-80 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch):	This instruction will freeze the display and suppress further response to changes of the BCD input.	
	«EL» on «0»	The display responds to the BCD input value.
	«EL» on «1»	The display freezes on the last value.
DP (Decimal Point):	The decimal point must be controlled externally. The module features an integral current limiting resistor.	
TTL logic:	«DP» on «0»	Decimal point on.
	«DP» on «1»	Decimal point off
CMOS-Logic:	«DP» on «0»	Decimal point off
	«DP» on «1»	Decimal point on

Truth table CMOS-Logic

Inputs							Outputs
EL	LT	D 2^3	C 2^2	B 2^1	A 2^0	BI	Display
x	0	x	x	x	x	x	8 (Test)
x	1	x	x	x	x	0	none
0	1	0	0	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	0	1	0	1	2
0	1	0	0	1	1	1	3
0	1	0	1	0	0	1	4
0	1	0	1	0	1	1	5
0	1	0	1	1	0	1	6
0	1	0	1	1	1	1	7
0	1	1	0	0	0	1	8
0	1	1	0	0	1	1	9
1	1	x	x	x	x	1	stored *

x = «0» or «1»

* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Truth table TTL logic

Inputs							Outputs	
EL	RBI	D 2^3	C 2^2	B 2^1	A 2^0	BI**	RBO	Display
x	x	x	x	x	x	0	0	none
0	0	0	0	0	0	x	0	none
0	1	0	0	0	0	1	1	0
0	x	0	0	0	1	1	1	1
0	x	0	0	1	0	1	1	2
0	x	0	0	1	1	1	1	3
0	x	0	1	0	0	1	1	4
0	x	0	1	0	1	1	1	5
0	x	0	1	1	0	1	1	6
0	x	0	1	1	1	1	1	7
0	x	1	0	0	0	1	1	8
0	x	1	0	0	1	1	1	9
0	x	1	0	1	0	1	1	A
0	x	1	0	1	1	1	1	b
0	x	1	1	0	0	1	1	C
0	x	1	1	0	1	1	1	d
0	x	1	1	1	0	1	1	E
0	x	1	1	1	1	1	1	F
1	x	x	x	x	x	1	1	stored *

x = «0» or «1 »

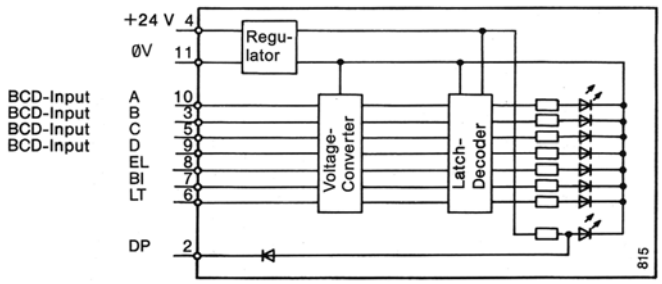
* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

** Input BI should only be shifted to «0» to obtain blanking of the display irrespective to the BCD input. Further information on this input is provided in the general section.

Type 815

- 7-segment display
- Memory
- BCD input
- Signal level adaptation
- 24 V supply voltage

Circuit diagram



In this module, the display is controlled with the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting incoming BCD signals.

Technical data

Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 61 mA
	= 24 V	typ. 36 mA
	= 30 V	typ. 30 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 20 kHz
	= 24 V	≤ 50 kHz
	= 30 V	≤ 50 kHz
Character height		16 mm
Depth behind panel		64 mm

Input data

All Inputs are connected to 0 V.

Input voltage all inputs

U_{in} «0»		min.	-3.5 V
or open to		max.	2 V
U_{in} «I»		min.	10 V
		max.	30 V

Input currents all inputs

I_{in} «0» with	U_{in} = -3.5 V	max.	-0.3 mA
	U_{in} = 2 V	max.	0.2 mA
I_{in} «1» with	U_{in} = 10 V	max.	1.5 mA
	U_{in} = 30 V	max.	3 mA

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor and a protective diode.

«DP» on «0» Decimal point off

«DP» on «1» Decimal point on
(+24 V) or open

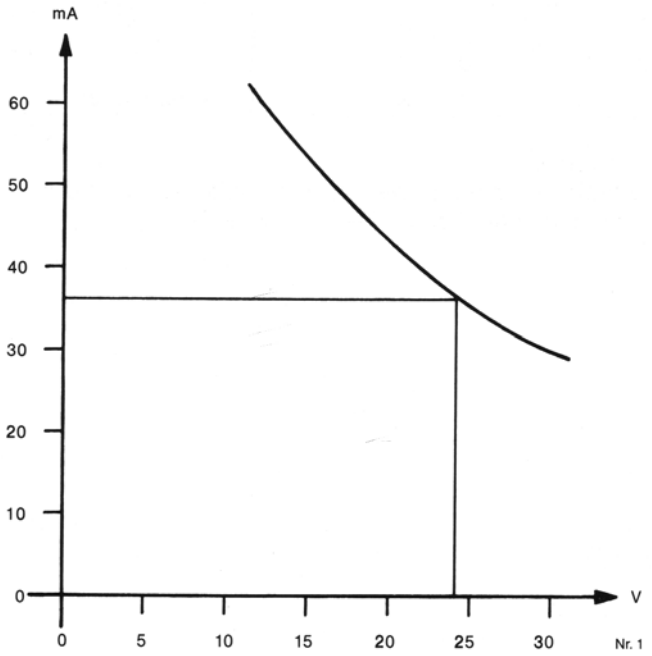
Truth table

Inputs							Outputs
LT	BI	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
0	1	x	x	x	x	x	8 (Test)
1	0	x	x	x	x	x	none
1	1	1	x	x	x	x	stored*

x = «0» or «1»

* controlled by applied BCD code during the leading edge of the «EL» instruction signal.

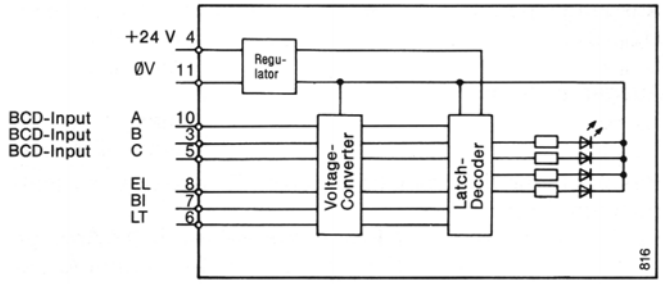
Supply current in relation to supply voltage



Type 816

- Sign and overflow display
- Memory
- BCD input
- 24 V supply voltage

Circuit diagram



This module is used to display sign and overflow (±1). It is controlled with the BCD code in positive logic.

The signal and display voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting incoming BCD signals.

Technical data

Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 30 mA
	= 24 V	typ. 18 mA
	= 30 V	typ. 16 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 20 kHz
	= 24 V	≤ 50 kHz
	= 30 V	≤ 50 kHz
Character height		16 mm
Depth behind panel		64 mm

Input data

All Inputs are connected to ground 0 V.

Input voltage (all inputs)

U_{in} «0»		min.	-3.5 V
or open to		max.	2 V
U_{in} «1»		min.	10 V
		max.	30 V

Input currents (all inputs)

I_{in} «0» with	U_{in} = -3.5 V	max.	-0.3 mA
	U_{in} = 2 V	max.	0.2 mA
I_{in} «1» with	U_{in} = 10 V	max.	1.5 mA
	U_{in} = 30 V	max.	3 mA

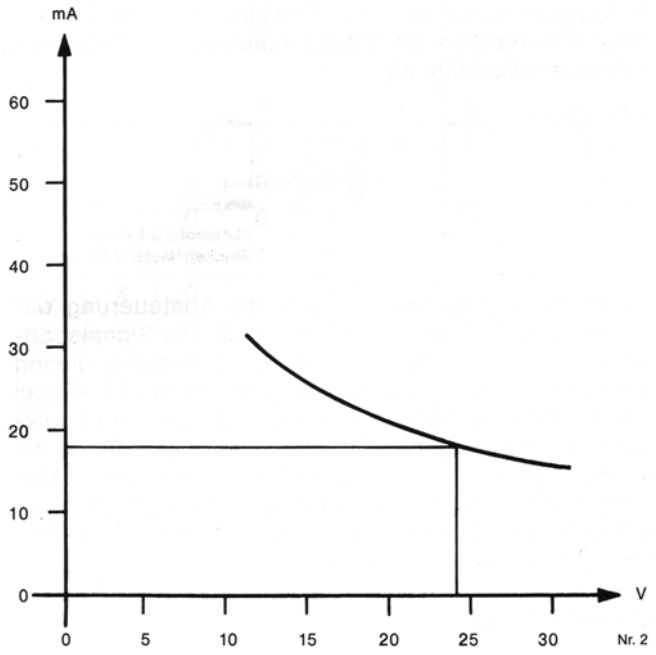
Truth table

Inputs						Outputs
LT	BI	C 2^2	B 2^1	A 2^0	EL	Display
1	1	0	0	0	0	+1
1	1	0	0	1	0	–
1	1	0	1	0	0	1
1	1	0	1	1	0	-1
1	1	1	0	0	0	+
1	1	1	0	1	0	+1
1	1	1	1	0	0	+1
1	1	1	1	1	0	–
0	1	x	x	x	x	±1 (Test)
1	0	x	x	x	x	none
1	1	x	x	x	1	stored *

x = «0» or «1»

* = controlled by applied BCD code during the leading edge of the «EL» instruction signal.

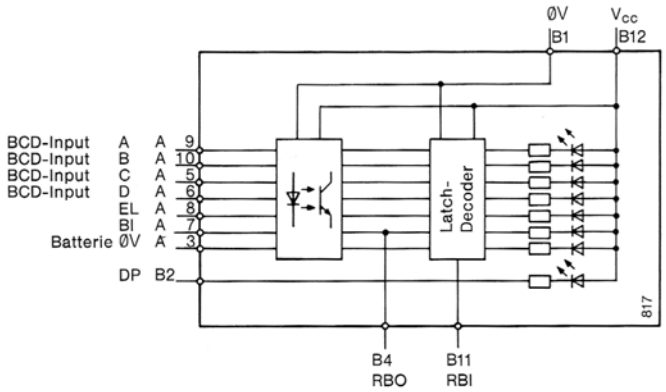
Supply current in relation to supply voltage



Type 817

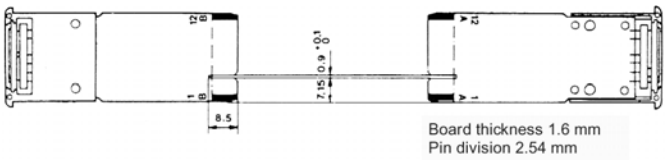
- 7-segment display
- BCD input
- Memory
- Galvanic separation
- 48 V signal voltage
- 5 V supply voltage

Circuit diagram



Caution

The circuit board thickness deviates from the standard thickness. The device is coded to prevent false insertion. The pins have a numbering scheme which deviates from the standard scheme.



The display in this module is controlled by the BCD code with positive logic. The signal voltage is 48 V. The built-in level transformer matches the 48 V signals to the TTL level and provides electric insulation. In the signal feedback path, a diode protects the optocoupler against destruction due to accidental pole reversal. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD signals.

Technical data

Supply voltage U_{CC}	+5 V ±5 %
Supply current I_{CC}	typ. 150 mA
Signal voltage	+48 V ±10 %
Limit frequency	≤ 40 kHz
Insulation voltage signal input/logic	typ. 2500 V DC
Character height	16 mm
Depth behind panel	74 mm

Input data

Input voltage

BCD input EL, BI

U_{in} «0»	max.	37 V
U_{in} «1»	min.	39.5 V
	max.	53 V

Input RBI

U_{in} «0»	max.	0.8 V
U_{in} «1»	min.	2 V
	max.	5 V

Input currents

BCD input EL, BI

I_{in} «0» with U_{in} = 37 V	max.	3 mA
I_{in} «1» with U_{in} = 48 V	max.	17 mA

Input RBI

I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	40 µA

Output data (Output RBO)

Output voltage

U_{out} «0»	max.	0.4 V
U_{out} «1»	min.	2.4 V

Output current

I_{out} «0»	max.	8 mA
I_{out} «1»	max.	-200 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch): This instruction will freeze the display and suppress further response to changes of the BCD input.

- «EL» on «0» The display responds to the BCD input value.
- «EL» on «1» The display freezes on the last value.

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor.

- «DP» on «0» Decimal point on
- «DP» on «1» Decimal point off

Truth table

Inputs							Outputs	
EL	D 2^3	C 2^2	B 2^1	A 2^0	RBI*	BI	RBO	Display
x	x	x	x	x	x	1	0	none
0	0	0	0	0	0	x	0	none
0	0	0	0	0	1	0	1	0
0	0	0	0	1	x	0	1	1
0	0	0	1	0	x	0	1	2
0	0	0	1	1	x	0	1	3
0	0	1	0	0	x	0	1	4
0	0	1	0	1	x	0	1	5
0	0	1	1	0	x	0	1	6
0	0	1	1	1	x	0	1	7
0	1	0	0	0	x	0	1	8
0	1	0	0	1	x	0	1	9
0	1	0	1	0	x	0	1	A
0	1	0	1	1	x	0	1	b
0	1	1	0	0	x	0	1	C
0	1	1	0	1	x	0	1	d
0	1	1	1	0	x	0	1	E
0	1	1	1	1	x	0	1	F
1	x	x	x	x	x	0	1	stored *

x = «0» or «1»

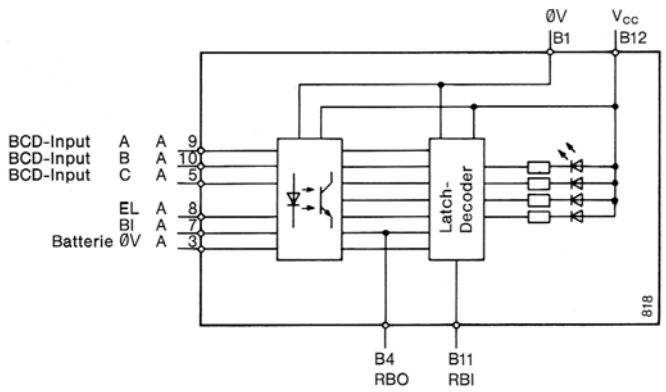
* May be controlled only by TTL level!

** controlled by applied BCD code during the leading edge of the «EL» instruction signal.

Type 818

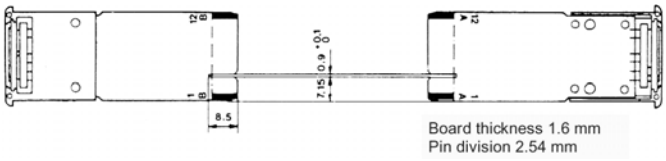
- Sign and overflow display
- BCD input
- Memory
- Galvanic separation
- 48 V signal voltage
- 5 V supply voltage

Circuit diagram



Caution

The circuit board thickness deviates from the standard thickness. The device is coded to prevent false insertion. The pins have a numbering scheme which deviates from the standard scheme.



The display in this module is controlled by the BCD code with positive logic. The signal voltage is 48 V. The built-in level transformer matches the 48 V signals to the TTL level and provides electric insulation. In the signal feedback path, a diode protects the optocoupler against destruction due to accidental pole reversal. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD signals.

Technical data

Supply voltage U_{CC}	+5 V ±5 %
Supply current I_{CC}	typ. 110 mA
Signal voltage	+48 V ±10 %
Limit frequency	≤ 40 kHz
Insulation voltage signal input/logic	typ. 2500 V DC
Character height	16 mm
Depth behind panel	74 mm

Input data

Input voltage

BCD input EL, BI

U_{in} «0»	max.	37 V
U_{in} «1»	min.	39.5 V
	max.	53 V

Input RBI

U_{in} «0»	max.	0.8 V
U_{in} «1»	min.	2 V
	max.	5 V

Input currents

BCD input EL, BI

I_{in} «0» with	U_{in} =	37 V	max.	3 mA
I_{in} «1» with	U_{in} =	48 V	max.	17 mA

Input RBI

I_{in} «0» with	U_{in} =	0.4 V	max.	-1.6 mA
I_{in} «1» with	U_{in} =	2.4 V	max.	40 µA

Output data (Output RBO)

Output voltage

U_{out} «0»	max.	0.4 V
U_{out} «1»	min.	2.4 V

Output current

I_{out} «0»	max.	8 mA
I_{out} «1»	max.	-200 µA

Description of Enable Latch (EL) and Decimal Point (DP):

EL (Enable Latch): This instruction will freeze the display and suppress further response to changes of the BCD input.

«EL» on «0» The display responds to the BCD input value.

«EL» on «1» The display freezes on the last value.

Truth table

Inputs						Outputs	
EL	RBI*	C 2^2	B 2^1	A 2^0	BI	RBO	Display
x	x	x	x	x	1	0	none
0	0	0	0	0	x	0	none
0	1	0	0	0	0	1	+1
0	x	0	0	1	0	1	–
0	x	0	1	0	0	1	1
0	x	0	1	1	0	1	-1
0	x	1	0	0	0	1	+
0	x	1	0	1	0	1	+1
0	x	1	1	0	0	1	+1
0	x	1	1	1	0	1	–
1	x	x	x	x	0	1	stored*

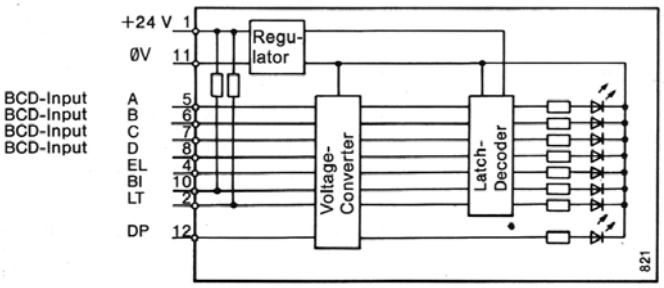
x = «0» or «1»

* May be controlled only by TTL level!

Type 821

- 7-segment display
- Memory
- BCD input
- Signal level adaptation
- 24 V signal and supply voltage

Circuit diagram



In this module, the display is controlled by the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD signals. Inputs «BI» and «LT» are already connected to the 24 V power supply via internal resistors. If these inputs are not used, the module will function properly due to these resistors. Both of these inputs must be controlled in open collector circuits.

Technical data

Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 52 mA
	= 24 V	typ. 32 mA
	= 30 V	typ. 28 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 10 kHz
	= 24 V	≤ 15 kHz
	= 30 V	≤ 20 kHz
Character height		16 mm
Depth behind panel		74 mm

Input data:

Input voltage all inputs (except DP)

U_{in} «0»	min.	-3.5 V
or open to	max.	2 V
U_{in} «1»	min.	10 V
	max.	30 V

Input voltage Input DP

U_{in} «0»	min.	-3.5 V
to	max.	0.7 V
U_{in} «1»	min.	1.1 V
	max.	30 V
	or open	

Input currents all inputs (except BI, LT and DP)

I_{in} «0» with	U_{in} =	-3.5 V	max. -150 µA
		2 V	max. 140 µA
I_{in} «1» with	U_{in} =	10 V	max. 700 µA
		30 V	max. 2.6 mA

Input currents inputs LT, BI

Pull-up resistances			3.3 kΩ
I_{in} «0» with	U_{in} =	-3.5 V	max. -11 mA
		2 V	max. -9.2 mA
I_{in} «1» with	U_{in} =	10 V	max. -7.2 mA
		30 V	max. 3 mA

Input currents input DP

I_{in} «0» with	U_{in} =	-3.5 V	max. -1 mA
		0.7 V	max. -400 µA
I_{in} «1» with	U_{in} =	1.1 V	max. -10 µA
		30 V	max. 1 µA

DP (Decimal point): «DP» on «0» Decimal point on
«DP» on «1» Decimal point off
(+24 V or open)

Truth table

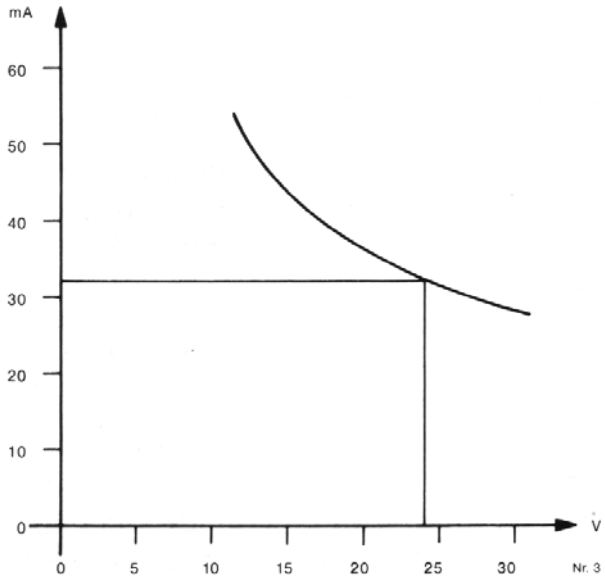
Inputs							Outputs
LT*	BI*	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	0	0
1	1	0	0	0	0	1	1
1	1	0	0	0	1	0	2
1	1	0	0	0	1	1	3
1	1	0	0	1	0	0	4
1	1	0	0	1	0	1	5
1	1	0	0	1	1	0	6
1	1	0	0	1	1	1	7
1	1	0	1	0	0	0	8
1	1	0	1	0	0	1	9
0	1	x	x	x	x	x	8 (Test)
1	0	x	x	x	x	x	none
1	1	1	x	x	x	x	stored**

x = «0» or «1»

* Inputs BI and LT are internally wired to H. An open collector control circuit is needed.

** controlled by applied BCD code during the leading edge of the «EL» instruction signal.

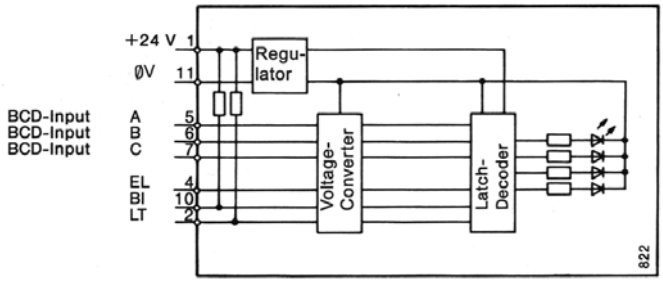
Supply current in relation to supply voltage



Type 822

- Sign and overflow display
- BCD input
- Signal level adaptation
- Memory
- 24 V signal and supply voltage

Circuit diagram



This module is used to display sign and overflow (± 1). It is controlled by the BCD code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming BCD signals. Inputs «BI» and «LT» are already connected to the 24 V power supply via internal resistors. If these inputs are not used, the module will function properly due to these resistors. Both of these inputs must be controlled in open collector circuits.

Technical data

Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 26 mA
	= 24 V	typ. 19 mA
	= 30 V	typ. 18 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 10 kHz
	= 24 V	≤ 15 kHz
	= 30 V	≤ 20 kHz
Character height		16 mm
Depth behind panel		74 mm

Input data

Input voltage all inputs

U_{in} «0»	min.	- 3.5 V
or open to	max.	2 V
U_{in} «1»	min.	10 V
	max.	30 V

Input currents all inputs (except BI and LT)

I_{in} «0» with U_{in} = -3.5 V		max. -150 µA
U_{in} = 2 V		max. 140 µ□A
I_{in} «1» with U_{in} = 10 V		max. 700 µ□A
I_{in} «0» with U_{in} = 30 V		max. 2.6 mA

All Inputs are connected to ground 0 V.

Input currents inputs LT, BI

Pull-up resistances		3.3 kΩ
I_{in} «0» with	U_{in} = -3.5 V	max. -11 mA
	U_{in} = 2 V	max. -9.2 mA
I_{in} «1» with	U_{in} = 10 V	max. -7.2 mA
	U_{in} = 30 V	max. 3 mA

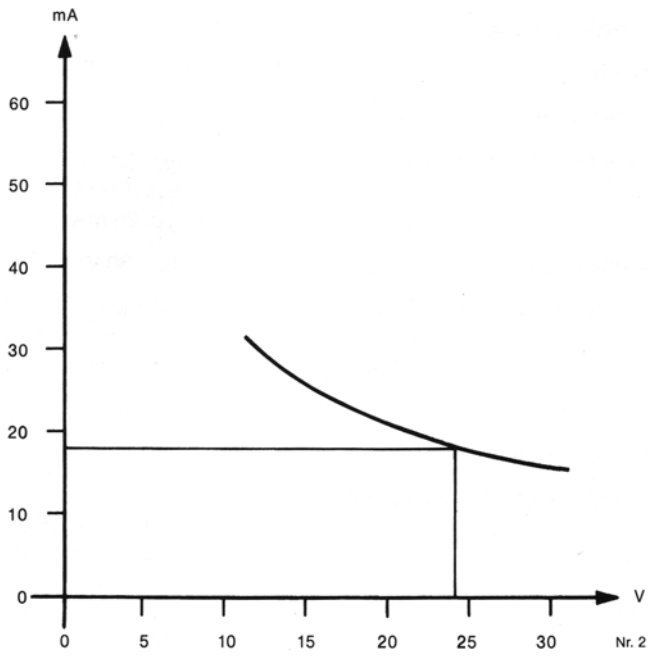
Truth table

Inputs						Outputs
LT*	BI*	EL	C 2^2	B 2^1	A 2^0	Display
1	1	0	0	0	0	+1
1	1	0	0	0	1	–
1	1	0	0	1	0	1
1	1	0	0	1	1	-1
1	1	0	1	0	0	+
1	1	0	1	0	1	+1
1	1	0	1	1	0	+1
1	1	0	1	1	1	–
1	1	0	0	0	0	+1
1	1	0	0	0	1	–
0	1	x	x	x	x	±1 (Test)
1	0	x	x	x	x	none
1	1	1	x	x	x	stored

x = «0» or «1 »

* Inputs BI and LT are internally wired to H. An open collector control circuit is needed.

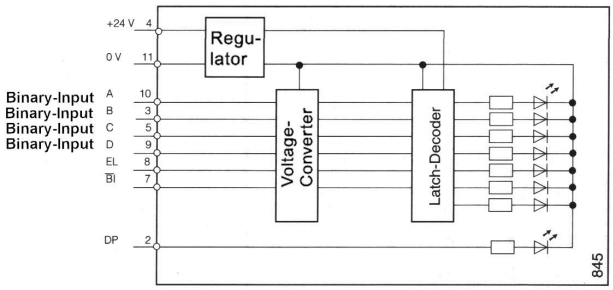
Supply current in relation to supply voltage



Type 845

- 7-segment display
- Memory
- Binary input
- Signal level adaptation
- 24 V signal and supply voltage

Circuit diagram



In this module, the display is controlled by the Binary Code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming Binary Code signals.

Technical data

Supply voltage V_{CC}		12-30 V
Supply current I_{CC} with V_{CC}	= 12 V	typ. 41 mA
	= 24 V	typ. 25 mA
	= 30 V	typ. 21 mA
Signal voltage		10-30 V
Limit frequency with V_{CC}	= 12 V	≤ 20 kHz
	= 24 V	≤ 50 kHz
	= 30 V	≤ 50 kHz
Character height		16 mm
Depth behind panel		64 mm

Input data except DP

Input voltage (all inputs)

U_{in} «0»	min.	-3 V
	max.	5 V
	or open	
U_{in} «1 »	min.	10 V
	max.	30 V

Input currents all inputs

I_{in} «0» with U_{in} = -3.5 V	max.	-0.3 mA
U_{in} = 2 V	max.	0.2 mA
I_{in} «1» with U_{in} = 10 V	max.	1.5 mA
U_{in} = 30 V	max.	3 mA

Open inputs = logical «0»

Input resistance (all inputs) ≈ 20 kΩ

DP (Decimal Point): The decimal point must be controlled externally. The module features an integral current limiting resistor and a protective diode.

«DP» on «0» Decimal point off

«DP» on «1» Decimal point on

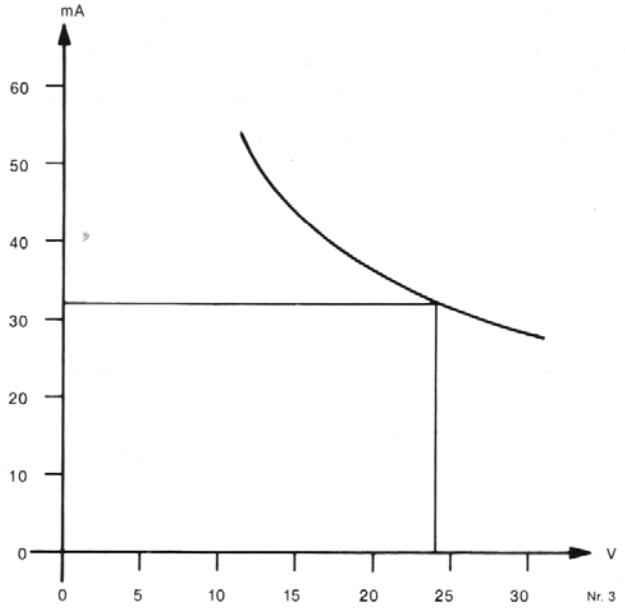
Truth table

Inputs						Outputs
$\overline{BI}$	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	0	0	0	0	0	0
1	0	0	0	0	1	1
1	0	0	0	1	0	2
1	0	0	0	1	1	3
1	0	0	1	0	0	4
1	0	0	1	0	1	5
1	0	0	1	1	0	6
1	0	0	1	1	1	7
1	0	1	0	0	0	8
1	0	1	0	0	1	9
1	0	1	0	1	0	A
1	0	1	0	1	1	b
1	0	1	1	0	0	C
1	0	1	1	0	1	d
1	0	1	1	1	0	E
1	0	1	1	1	1	F
0	x	x	x	x	x	none
1	1	x	x	x	x	stored*

x = «0» or «1»

* controlled by applied Binary Code during the leading edge of the «EL» instruction signal.

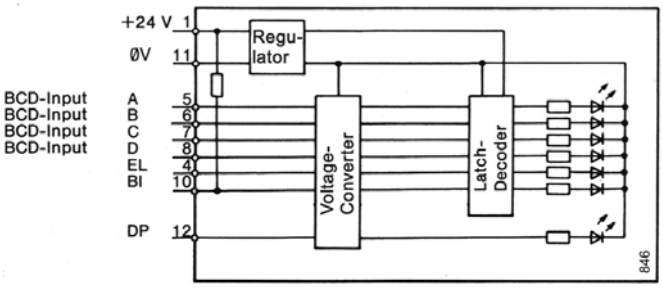
Supply current in relation to supply voltage



Type 846

- 7-segment display
- Memory
- Binary input
- Signal level adaptation
- 24 V signal and supply voltage

Circuit diagram



In this module, the display is controlled by the Binary Code in positive logic. The signal and supply voltage is +24 V. A control signal (input EL) makes it possible to freeze the display without affecting the incoming Binary Code signals. Input «BI» is already connected to the 24 V power supply via internal resistor. If this input is not used, the module will function properly due to this resistor. The input must be controlled in open collector circuits.

Technical data

Supply voltage V_{CC}			12-30 V
Supply current I_{CC} with	V_{CC} =	12 V	typ. 43 mA
		24 V	typ. 34 mA
		30 V	typ. 27 mA
Signal voltage			10-30 V
Limit frequency with	V_{CC} =	12 V	≤ 10 kHz
		24 V	≤ 15 kHz
		30 V	≤ 20 kHz
Character height			16 mm
Depth behind panel			74 mm

Input data

Input voltage all inputs (except DP)

U_{in} «0»		min.	-3.5 V or open
		max.	2 V
U_{in} «1»		min.	10 V
		max.	30 V

Input voltage input DP

U_{in} «0»		min.	-3.5 V
	to	max.	0.7 V
U_{in} «1»		min.	1.1 V
		max.	30 V or open

Input currents all inputs (except BI and DP)

I_{in} «0» with	U_{in} = -3.5 V	max.	-150 mA
	U_{in} = 2 V	max.	140 µA
I_{in} «1» with	U_{in} = 10 V	max.	700 µA
	U_{in} = 30 V	max.	2.6 mA

Input currents input BI

I_{in} «0» with	U_{in} = -3.5 V	max.	-11 mA
	2 V	max.	-9.2 mA
I_{in} «1» with	U_{in} = 10 V	max.	-7.2 mA
	30 V	max.	3 mA

Input currents input DP

I_{in} «0» with	U_{in} = -3.5 V	max.	-1 mA
	0.7 V	max.	-400 µA
I_{in} «1» with	U_{in} = 1.1 V	max.	-10 µA
	30 V	max.	1.6 µA

DP (Decimal point): «DP» on «0» Decimal point on
«DP» on «1» Decimal point off
(+24 V or open)

Truth table

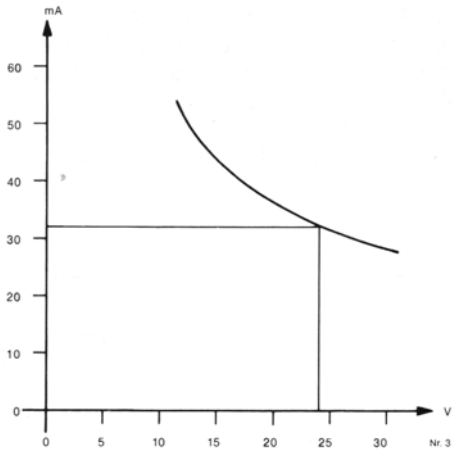
Inputs						Outputs
BI*	EL	D 2^3	C 2^2	B 2^1	A 2^0	Display
1	0	0	0	0	0	0
1	0	0	0	0	1	1
1	0	0	0	1	0	2
1	0	0	0	1	1	3
1	0	0	1	0	0	4
1	0	0	1	0	1	5
1	0	0	1	1	0	6
1	0	0	1	1	1	7
1	0	1	0	0	0	8
1	0	1	0	0	1	9
1	0	1	0	1	0	A
1	0	1	0	1	1	b
1	0	1	1	0	0	C
1	0	1	1	0	1	d
1	0	1	1	1	0	E
1	0	1	1	1	1	F
x	x	x	x	x	x	8 (Test)
0	x	x	x	x	x	none
1	1	x	x	x	x	stored**

x = «0» or «1»

* Input BI is internally wired to H. An open collector control circuit is needed.

** depends on the BCD value during the leading edge of the «EL».

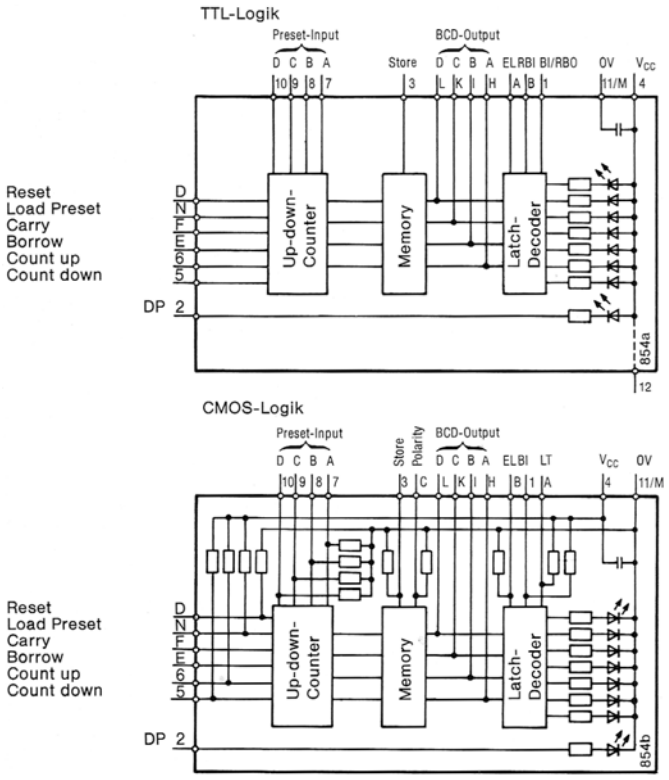
Supply current in relation to supply voltage



Type 854

- 7-segment display
- Up/down counting input
- Memory
- BCD output
- TTL or CMOS-Logic
- 5, 10, 12 or 15 V supply voltage

Circuit diagram



This module is a display unit with a pre-selectable up/down counter. The clock inputs for up and down counting are separated.

The counter can be preset to the value available at the inputs (Preset Input) in the BCD code via a signal (Load Preset input).

With the control signal (input store), it is possible to store the counter status at any given moment. This permits a stationary signal at the BCD output although the counter continues to operate.

The BCD output can be used for further signal processing. The «polarity» input makes it possible to control the «Store» instruction with the leading or trailing edge of the signal.

The second store instruction (Input EL) makes it possible to freeze the display.

In the CMOS model, all inputs are terminated with resistors.

Observe the General handling directions for CMOS logic elements (s. page **Fehler! Textmarke nicht definiert.**).

Technical data

Character height	16 mm
Depth behind panel	64 mm

		TTL	CMOS
Supply current I_{CC}	typ.	200 mA	80 mA
Signal flow times			
Clock display	max.	197 ns	1.52 ms
Clock carry/borrow	max.	26 ns	200 ns
Clock BCD output	max.	97 ns	590 ns
Load BCD output	max.	90 ns	680 ns
Load display	max.	190 ns	1.40 ms
Reset BCD output	max.	85 ns	470 ns
Store BCD output	max.	27 ns	310 ns
Store display	max.	127 ns	1.03 ms

Input data

Input voltage (all inputs)

		TTL	CMOS
U_{in} «0» with V_{CC} = 5 V	max.	0.8 V	1.5 V
= 10 V	max.		3 V
= 12 V	max.		3.6 V
= 15 V	max.		4.5 V
U_{in} «1» with V_{CC} = 5 V	min.	2 V	3.5 V
= 10 V			7 V
= 12 V			8.4 V
= 15 V			10.5 V

Input currents TTL logic:

All Inputs except EL, RBI, BI

I_{in} «0» with U_{in} = 0.4 V	max.	-0.6 mA
I_{in} «1» with U_{in} = 0.7 V	max.	20 µA

Inputs EL and RBI

I_{in} «0» with U_{in} = 0.4 V	max.	-1.6 mA
I_{in} «1» with U_{in} = 2.4 V	max.	40 µA

Input BI

I_{in} «0» with U_{in} = 0.4 V	max.	-3.2 mA

Input currents CMOS-Logic

Inputs Reset, EL, Store, Polarity and Preset

Pull-up/Pull-down resistances				100 kΩ
I_{in} «0» with	U_{in} =	1.5 V	max.	15.5 µA
		3 V	max.	31 µA
		3.6 V	max.	37 µA
		4.5 V	max.	46 µA
I_{in} «1» with	U_{in} =	3.6 V	max.	36 µA
		7 V	max.	71.5 µA
		8.4 V	max.	86 µA
		10.5 V	max.	107 µA

Inputs Count up, Count down, Load Preset, BI, LT

I_{in} «0» with	U_{in} =	1.5 V	max.	-36 µA
		3 V	max.	-71.5 µA
		3.6 V	max.	-86 µA
		4.5 V	max.	-107 µA
I_{in} «1» with	U_{in} =	3.6 V	max.	-15.5 µA
		7 V	max.	-31 µA
		8.4 V	max.	-37 µA
		10.5 V	max.	-46 µA

Output data

Output voltages
BCD output, Carry, Borrow, RBO (with TTL only)

		TTL	CMOS
U_{out} «0» with V_{CC}	= 5 V	max. 0.4 V	0.4 V
	= 10 V	max.	0.5 V
	= 12 V	max.	0.5 V
	= 15 V	max.	0.5 V
U_{out} «1» with V_{CC}	= 5 V	min. 2.4 V	4.5 V
	= 10 V		9.5 V
	= 12 V		11.5 V
	= 15 V		14.5 V

Output currents TTL logic:

BCD output
I_{out} «0» max. -6.4 mA
I_{out} «1» max. -360 µA

Carry/borrow
I_{out} «0» max. 8 mA
I_{out} «1» max. -400 µA

RBO
I_{out} «0» max. 3.2 mA
I_{out} «1» max. 80 µA

Output currents CMOS-Logic

All outputs

I_{out} «0» with V_{CC}	= 5 V	max. 0.8 mA
	= 10 V	max. 2 mA
	= 12 V	max. 2.5 mA
	= 15 V	max. 3.6 mA
I_{out} «1» with V_{CC}	= 5 V	max. -0.4 mA
	= 10 V	max. -1.4 mA
	= 12 V	max. -1.7 mA
	= 15 V	max. -2.2 mA

Description of functions:

«Count up»/ «count down«»
The trailing edge of the counting pulse is used for the counting operation. The count down input must be on «1» if the module is to count up. For down counting, the count up input must be on «1».

«Preset input»
This input is controlled with the BCD code. Each value from 0 to 9 can be applied. The «load preset» enters this value into the counter. From this value on, the counter will count up or down.

«Load preset»
A signal at this input makes it possible to set the counter to the value available at the «preset input».

«Load preset» on «1»
The counter is free

«Load preset» on «0»
The counter is set to the value applied.

«Reset»
With this input, the counter can be reset to zero at any time.

«Reset» on «0»
The counter is free

«Reset» on «1»
The counter is reset to zero

Caution:

«Load preset» and «Reset» should never be activated at the same time because this may damage the counter.

«Carry»/ «Borrow»
These outputs are used when several decades are needed (carryover). The «Carry» output is connected with the «Count up» input and the «Borrow» output with the «Count down» input of the next higher decade. During the transition from 9 to 0, and from 0 to 9, the module generates a «Carry» and a «Borrow» respectively. The length of the carryover pulse corresponds to the length of the counting pulses.

«Store»
This instruction is used to freeze the counter at a given point in time. When using several counting stages, all carryovers must be processed before the store instruction is initiated.

TTL logic:

«Store«» on «0»
Memory contents and BCD output are frozen.

«Store» on «1»
Memory contents and BCD output follow counter.

CMOS logic:

The store function depends on the signal at the «Polarity» input.

«Polarity» (For CMOS only)
A signal at this input controls the edge of the «Store» instruction.

«Polarity» on «0»
The storage process is initiated by the positive edge of the «Store» instruction.

«Polarity» on «1»
The storage process is initiated by the negative edge of the «Store» instruction.

EL (Enable Latch)
This instruction will freeze the display irrespective of the states f the counter and memory.

«EL» on «0»
The display follows to the BCD output value.

«EL» on «1»
The display freezes irrespective of the information from the counter and memory.

DP (Decimal Point)
The decimal point must be controlled externally. The module features an integral current limiting resistor.

TTL logic:

«DP» on «0» Decimal point on.
«DP» on «1» Decimal point off.

CMOS logic:

«DP» on «0» Decimal point off.
«DP» on «1» Decimal point on.

Truth table

Preset inputs				Load Preset	Display
D 2^3	C 2^2	B 2^1	A 2^0		
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	2
0	0	1	1	0	3
0	1	0	0	0	4
0	1	0	1	0	5
0	1	1	0	0	6 / b***
0	1	1	1	0	7
1	0	0	0	0	8 (Test)
1	0	0	1	0	9
x	x	x	x	1	count

Polarity	Store	BCD outputs
0	0	not stored
0	⌐	stored
1	1	not stored
1	⌙	stored

Inputs					Outputs					
						BCD outputs				Display
EL	RBI (nur TTL)	LT (nur CMOS)	Store (TTL)	BI	RBO	D 2^3	C 2^2	B 2^1	A 2^0	
x	x	0	x	1	1	x	x	x	x	8 (Test)
x	x	1	x	0	0	x	x	x	x	none
0	0	1	1	x	0	0	0	0	0	none
0	1	1	1	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	1	1
0	1	1	1	1	1	0	0	1	0	2
0	1	1	1	1	1	0	0	1	1	3
0	1	1	1	1	1	0	1	0	0	4
0	1	1	1	1	1	0	1	0	1	5
0	1	1	1	1	1	0	1	1	0	6 / b***
0	1	1	1	1	1	0	1	1	1	7
0	1	1	1	1	1	1	0	0	0	8
0	1	1	1	1	1	1	0	0	1	9
1	1	1	x	1	1	x	x	x	x	stored*
0	1	1	0	1	1					stored**

x = «1» or «1»

* controlled by the applied BCD code during the leading edge of the «EL» instruction signal.

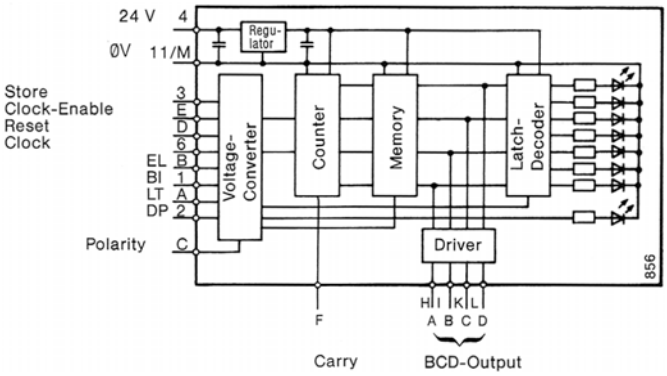
** Depends on the counter status before the trailing edge of the «Store» instruction.

*** The display for TTL logic is 6 and for CMOS logic, it is b.

Type 856

- 7-segment display
- Counting input
- Memory
- BCD output
- Driver
- 24 V signal and supply voltage

Circuit diagram



This module is a display unit with a counter and a memory.

The signal and supply voltage is +24 V.

With a control signal (input store), the counter status can be stored at any given time. This permits a stationary signal at the BCD output although the counter continues to operate.

The BCD output is wired to the PCB terminations in an open collector circuit.

The «polarity» input makes it possible to control the «Store» instruction with the leading or trailing edge of the signal.

Technical data

Supply voltage V_{CC}	18-27 V
Supply current I_{CC}	typ. 95 mA
Signal voltage	13.5-30 V
Limit frequency	≤ 100 kHz
Width of counting pulse	min. 1 µs
Character height	16 mm
Depth behind panel	74 mm

Input data

Input voltage (all inputs)

U_{in} «0»	max.	8 V
U_{in} «1»	min.	13.5 V
	max.	30 V

Input currents

I_{in} «0»	max.	2 µA
I_{in} «1»	max.	1.2 µA

Output data (Carry only)

Output voltage

U_{out} «0»	max.	2 V
U_{out} «1»	min.	13 V

Output current

I_{out} «0»	max.	-6 mA
I_{out} «1»	max.	6 mA

BCD output via driver (NPN):

Switching voltage	max.	30 V
Switching current	max.	300 mA
Driver loss power	max.	0.5 W
Saturation voltage with I_C=300 mA	max.	1.2 V

Description of functions:

«Clock»
The counting operation is controlled by the leading edge of the pulse. If several decades are switched together, all «Clock» inputs must be wired together.

«Clock Enable»
This input is used to enable or disable the counter. In the lowest decade, it is set to «1». In an assembly of several decades, it must be wired to the «carry» output of the next lower decade.

«Clock Enable» on «0»
The counter is blocked..

«Clock Enable» on «1»
The counter is free.

«Reset»
With this input, the counter can be reset to zero at any time.

«Reset» on «0»
The counter is free

«Reset» on «1»
The counter is reset to zero

«Carry»
This input is used when several decades are needed (carryover). The «Carry» output is connected with the «clock enable» input of the next higher decade. During the transition from 9 to 0, the module generates a pulse.

«Store»
This instruction is used to freeze the counter at a given point in time. When using several counting stages, all carryover must be processed before the store instruction is initiated. The «Store» function depends on the signal at the «Polarity» input.

«Polarity»
A signal at this input controls the edge of the «Store» instruction.

«Polarity» on «0»
The storage process is initiated by the positive edge of the «Store» instruction.

«Polarity» on «1»
The storage process is initiated by the negative edge of the «Store» instruction.

Enable Latch «EL» This instruction will freeze the display irrespective of the states f the counter and memory.

«EL» on «0»
The display follows to the BCD output value.

«EL» on «1»
The display freezes irrespective of the information from the counter and memory.

DP (Decimal Point) The decimal point must be controlled externally. The module features an integral current limiting resistor.

«DP» on «0» Decimal point off.

«DP» on «1» Decimal point on.

Truth table

Polarity	Store	BCD-Outputs
0	0	not stored
0	⌐	stored
1	1	not stored
1	¬	stored

Inputs			Outputs				
			BCD-Outputs				Display
EL	LT	BI	D 2^3	C 2^2	B 2^1	A 2^0	
x	x	0	x	x	x	x	none
x	0	1	x	x	x	x	8 (Test)
0	1	1	0	0	0	0	0
0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	2
0	1	1	0	0	1	1	3
0	1	1	0	1	0	0	4
0	1	1	0	1	0	1	5
0	1	1	0	1	1	0	6
0	1	1	0	1	1	1	7
0	1	1	1	0	0	0	8
0	1	1	1	0	0	1	9
1	1	1	x	x	x	x	stored*

x = «1» or «1»

* controlled by the applied BCD code during the leading edge of the «EL» instruction.